BAT32G439 Datasheet

High-performance 32-bit microcontrollers based on ARM® V8-M architecture STAR-MC1 processors

Built-in 256KB Flash, intergrated rich analog functions, timers and various communication interfaces

V0.1.4

Features

- **Core:**
  - ARM® V8-M architecture STAR-MC1 core, 3-stage pipelined 32-bit processor, balanced and optimized for performance and power consumption
  - 8KB instruction cache, 4KB data cache
  - Memory protection unit supporting 8 regions
  - 8 interrupt priority levels support up to 240 interrupt requests
  - Operating frequency: 32KHz to 128MHz
- **Operations:**
  - Built-in Digital Signal Processing Unit (DSP), supports SIMD's DSP-enhanced instructions
  - Floating-point unit (FPU) with tenfold performance improvement, supporting single-precision conversions, addition, subtraction, multiplication, totalization and square root operations
  - Hardware divider (integer division instructions delayed within 2 to 11 cycles) and single-cycle multiplier
- **Digital filter:**
  - Built-in a 2-channel 2nd order digital filter (IIR) that can be cascaded as the 4th order filter
- **Memory:**
  - 256KB flash memory with shared program and data storage
  - 4KB dedicated data flash memory
  - 64KB SRAM memory +2KB backup SRAM with parity check
- **Ultra low power operating environment:**
  - Supply voltage range: 2.5V to 5.5V
  - Temperature range: -40°C to 105°C
  - Low power modes: sleep mode, deep sleep mode, and deep sleep mode with partial power down support
  - Operating power consumption: 100μA/MHz @128MHz
  - Power consumption in deep sleep mode: 150μA
  - Deep sleep mode + 32.768K + RTC operation: 155μA
  - Power consumption in deep sleep mode with partial power down: 20μA
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
- **Input/output ports:**
  - I/O ports: 83x
  - Capable of N-channel open drain, internal pull-up, and internal pull-down switching
  - Built-in key interrupt detection
  - Built-in control circuit for clock output/buzzer output
- **Debugging Interface:**
  - Serial two-wire debugger (SWD)
  - JTAG port debugger
- **Timers:**
  - General-purpose PWM timer: 32bit 4-channel GPT0 unit, 16bit 8-channel GPT1 unit (support BLDC-controlled PWM waveform generation, etc.)
  - 16-bit timer: 8 channels x 2 units
  - 15-bit interval timer: 1x
  - Real time clock (RTC): 1x (with perpetual calendar, alarm function, and support a wide range of clock correction)
  - Watchdog timer: 2x (IWDT+WWDT)
  - SysTick timer: 1x (24bit, can select from F_{CLK} or F_{IL})
- **Rich and flexible interfaces:**
  - 4-channel serial communication unit: each channel can be freely configured as 1-channel standard UART, 2-channel SPI, or 2-channel simplified I^2C.
  - Standard SPI: 2 channels (support 8bit and 16bit)
  - QSPI: 1 channel, supports data encryption
  - Standard I^2C: 2 channels
  - LIN bus: 1 channel
  - CAN: 2 channels
  - IrDA: 1 channel
  - LCD bus interface: support interfaces 8080 and 6800
- **Safety features:**
  - AES advanced encryption engine, support AES standard data encryption and decryption operations, the key length can be 128bit, 256bit
  - True random number generator TRNG, generating 32-bit random numbers
  - Conform to IEC/UL 60730 and EC61508 standards
  - Report abnormal storage access errors

- Built-in voltage detection (LVD) circuit (settable threshold voltage)

- **Clock management:**
  - Built-in a high-speed oscillator with accuracy of ±1%, supporting 2MHz to 64MHz system clocks and peripheral module operation clocks
  - Built-in a PLL with a high-precision oscillator can provide 24MHz to 128MHz system clocks and peripheral module operation clocks.
  - Built-in a 30KHz/15KHz low-speed oscillator
  - Support 1MHz to 20MHz external crystal oscillators, support off-oscillation monitoring
  - Support 32.768KHz external crystal oscillator, which can be used to calibrate the on-chip high-speed oscillator.
- **Enhanced DMA controller:**
  - Interrupt trigger start
  - Selectable transfer modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode)
  - Transfer source/destination realm are selectable from the full address space range
- **Linkage controller:**
  - It can link event signals to realize the linkage of peripheral functions
  - 163 input events and 33 trigger events
- **Rich analog peripherals:**
  - 12-bit ADC converter unit 3, ADC0 8-channel, ADC1 8-channel, ADC2 16-channel, support a total of 32 external analog channels, conversion rate of 1.42Msps @ 64MHz, internally selectable PGA outputs as conversion channels, with temperature sensor(s), support for single-channel conversion mode and 2, 3, 4-channel scanning conversion mode
  - 8-bit D/A converter, 2-channel analog output, real-time output function, output voltage range: 0~V_{DD}
  - Comparator (CMP), built-in a four-channel comparator with selectable input sources, and the reference voltage can be selected from the external reference voltage or the internal reference voltage
  - Programmable Gain Amplifier (PGA) with a built-in four-channel PGA with an external GND pin (can be used as differential mode)
  - Support SFR guard and avoid misoperation
  - Support RAM parity check
  - Support hardware CRC
  - A/D test function
  - Digital output signal level detection function for input/output pins
  - 128-bit unique ID number
  - Flash Level 2 protection in the debug mode (Level1: only perform flash full-scale erase, cannot be read or written. Level2: Emulator connection is invalid, cannot operate on flash.)

- **Package:**
  - Support 64Pin, 80Pin, and 100Pin packages.

1 Overview

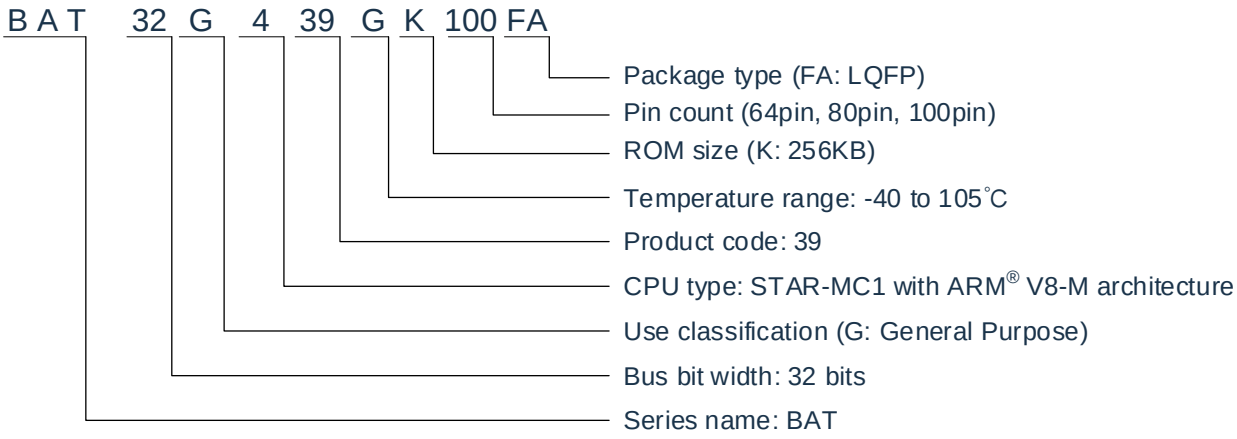
1.1 Brief introduction

The BAT32G439 microcontroller, based on the high-performance ARM® V8-M architecture with a 32-bit RISC core, operates at up to 128MHz. It features high-speed embedded flash memory (up to 256KB for program/data storage) and up to 64KB of SRAM. The product integrates multiple standard interfaces including I²C, SPI, UART, IrDA, LIN, QSPI, CAN bus, and LCD bus. It includes a 12-bit A/D converter, temperature sensors, an 8-bit D/A converter, comparators, and a programmable gain amplifier. The 12-bit A/D converter can capture signals from external sensors and works in conjunction with the internal programmable gain amplifier, reducing system design costs. The 8-bit D/A converter is suitable for audio playback or power control. An integrated temperature sensor enables real-time environmental monitoring. The built-in comparators support both high-speed and low-speed modes, useful for motor control feedback and battery monitoring, respectively. Advanced timer modules include a SysTick timer, a 16-channel 16-bit timer, a 15-bit interval timer, a watchdog timer, and a real-time clock. It features a 4-channel 32-bit and an 8-channel 16-bit general-purpose PWM timer, supporting complex control functions for products like DC brushless motors. Safety features include an AES encryption engine, true random number generator, DSP, and FPU computation units, meeting requirements for IoT devices in real-time control and digital signal processing.

The BAT32G439 excels in low-power performance with support for sleep and deep sleep modes, consuming 100μA/MHz @128MHz during operation and only 20μA in deep sleep mode with power-down hold, making it ideal for battery-powered devices. Furthermore, it includes an event-link controller enabling direct hardware module connection without CPU intervention, enhancing response speed and extending battery life by reducing CPU activity.

These features make the BAT32G439 microcontroller series suitable for various applications including automotive body control, motor drive control, home appliances, mobile devices, and IoT devices, emphasizing high performance and low power consumption.

1.2 Product model list



BAT32G439 product list:

Pin count	Package	Product name
64 pins	64-pin plastic package LQFP (10X10mm, 0.5mm pitch)	BAT32G439GK64FA
80 pins	80-pin plastic package LQFP (12X12mm, 0.5mm pitch)	BAT32G439GK80FA
100 pins	100-pin plastic package LQFP (14X14mm, 0.5mm pitch)	BAT32G439GK100FA

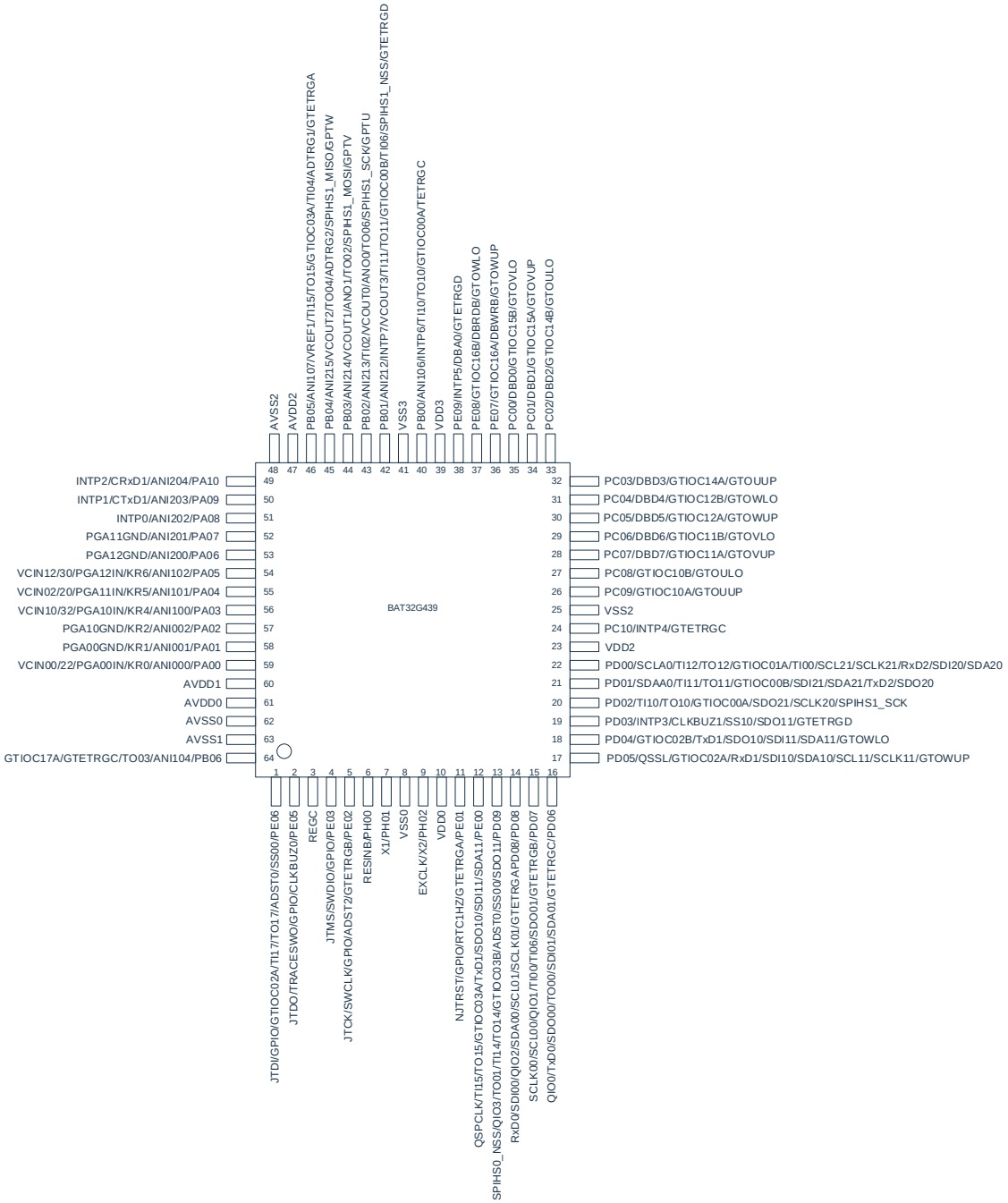
FLASH, SRAM memory:

Flash memory	Dedicated data Flash memory	SRAM	BAT32G439		
			64 pins	80 pins	100 pins
256KB	4KB	64KB	BAT32G439GK64	BAT32G439GK80	BAT32G439GK100

1.3 Top view

1.3.1 BAT32G439GK64FA

- 64-pin plastic package LQFP (10x10mm, 0.5mm pitch)



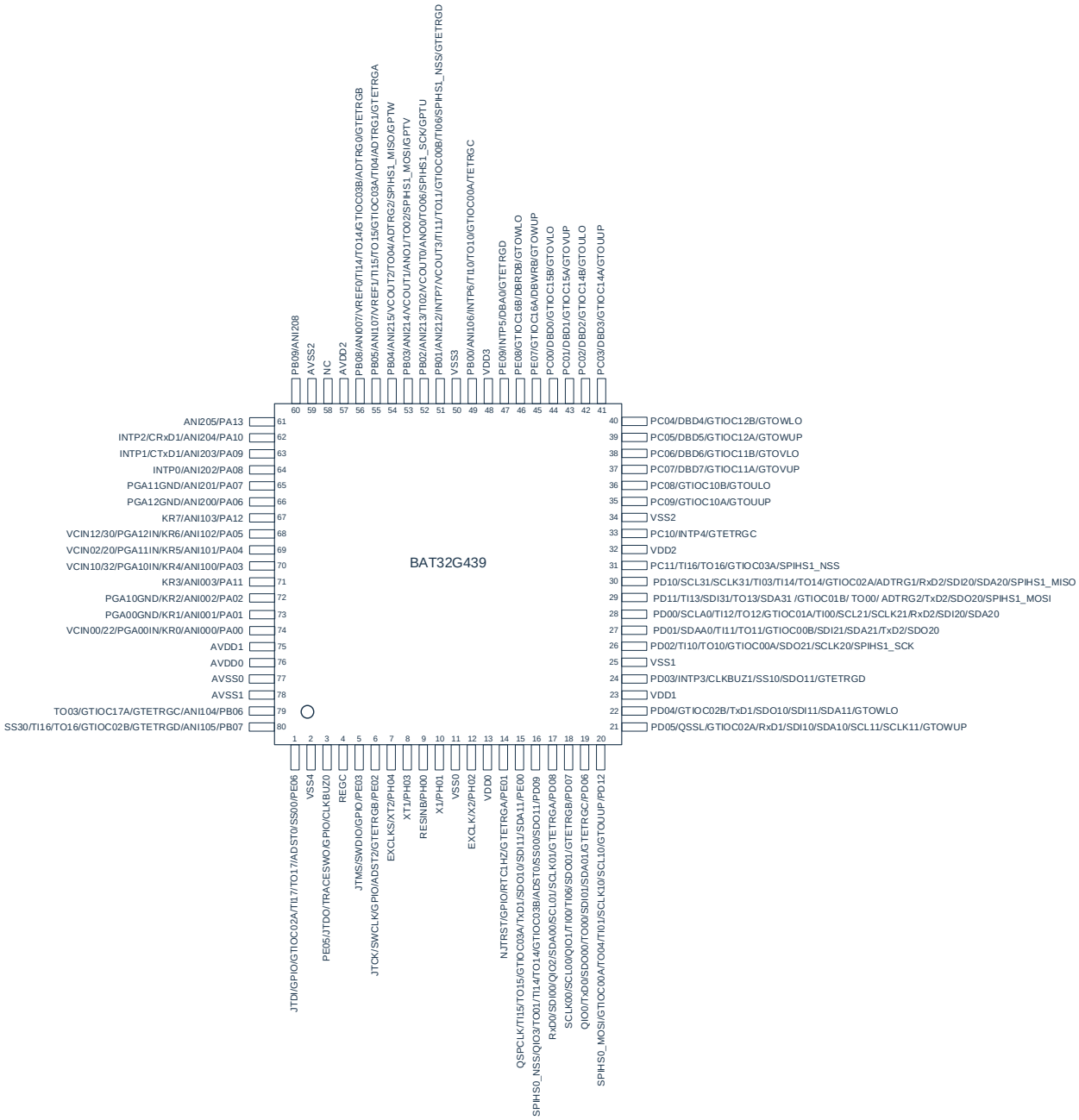
Note1: The AV_{SS0}, AV_{SS1}, AV_{SS2} pins and the V_{SS0}, V_{SS2}, V_{SS3} pins must be at the same potential.

Note2: The voltage at each AV_{DD0}, AV_{DD1}, AV_{DD2} pin must be equal to the voltage at the V_{DD0}, V_{DD2}, V_{DD3} pins.

Note3: The AV_{DD0}, AV_{DD1}, AV_{DD2} pins and V_{DD0}, V_{DD2}, V_{DD3} pins must be connected to the power supply.

1.3.2 BAT32G439GK80FA

- 80-pin plastic package LQFP (12x12mm, 0.5mm pitch)



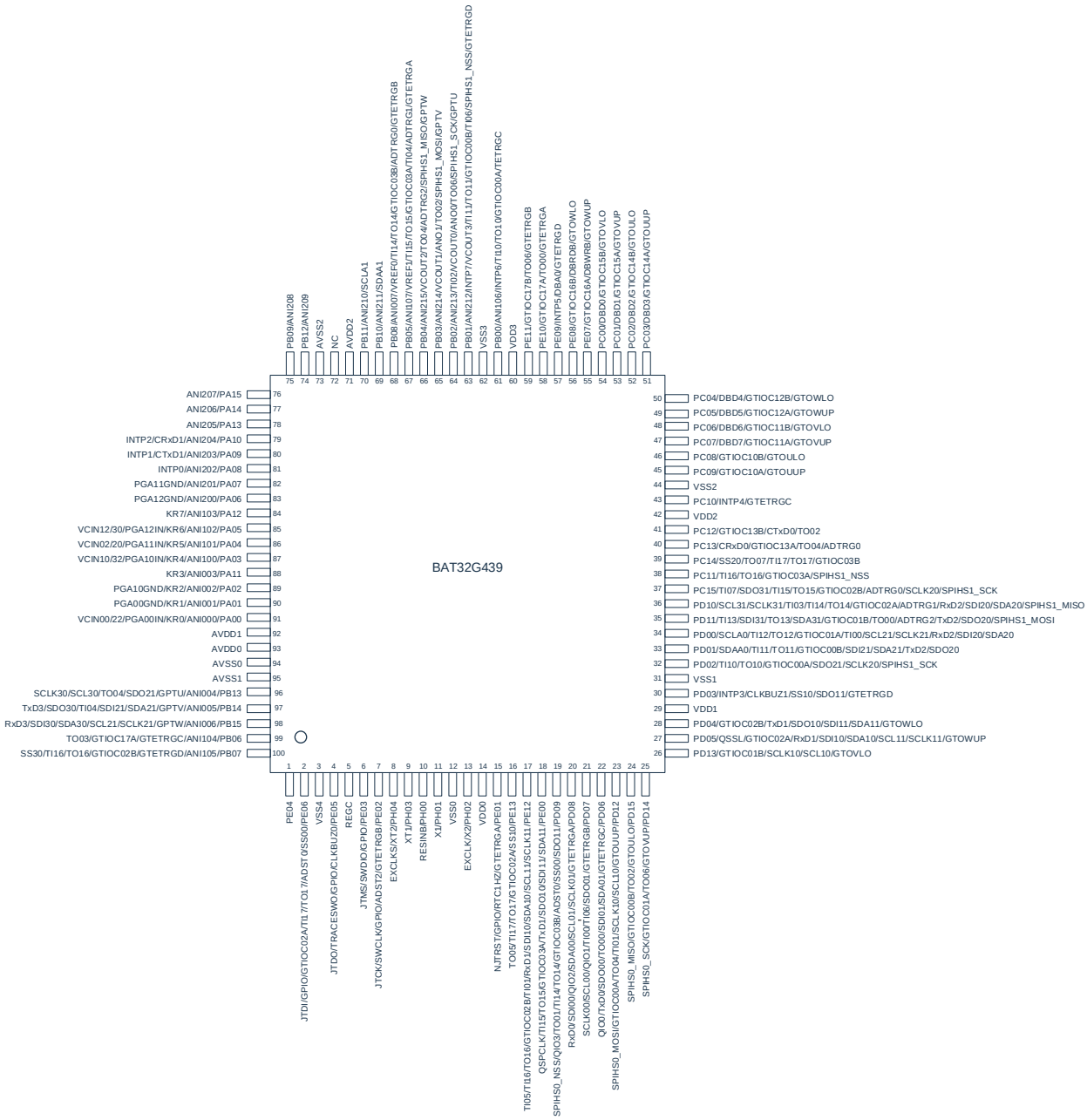
Note1: The AV_{SS0}, AV_{SS1}, AV_{SS2} pins and the V_{SS0}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4} pins must be at the same potential.

Note2: The voltage at each AV_{DD0}, AV_{DD1}, AV_{DD2} pin must be equal to the voltage at the V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3} pins.

Note3: The AV_{DD0}, AV_{DD1}, AV_{DD2} pins and V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3} pins must be connected to the power supply.

1.3.3 BAT32G439GK100FA

- 100-pin plastic package LQFP (14x14mm, 0.5mm pitch)

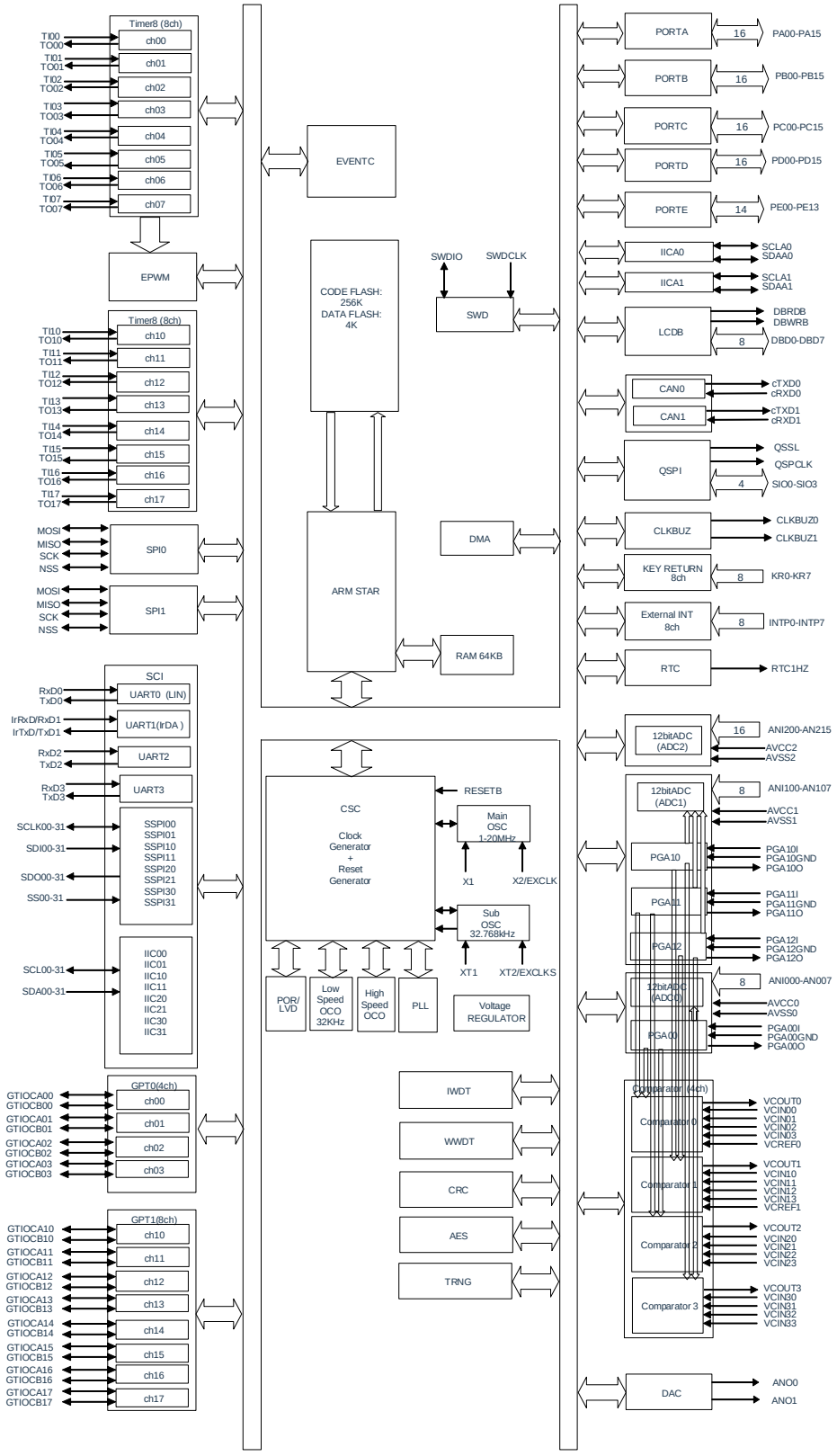


Note1: The AV_{SS0}, AV_{SS1}, AV_{SS2} pins and the V_{SS0}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4} pins must be at the same potential.

Note2: The voltage at each AV_{DD0}, AV_{DD1}, AV_{DD2} pin must be equal to the voltage at the V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3} pins.

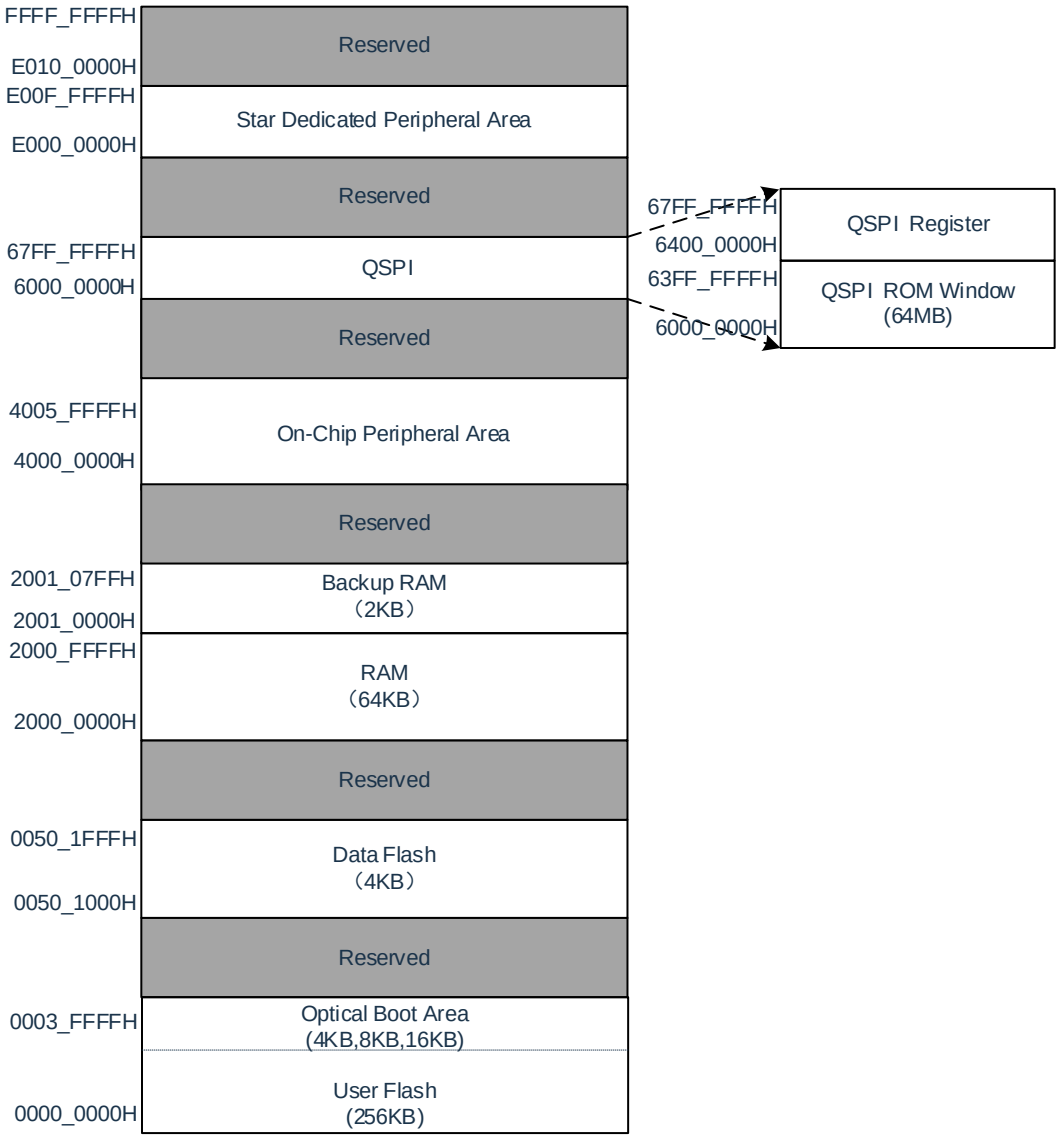
Note3: The AV_{DD0}, AV_{DD1}, AV_{DD2} pins and V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3} pins must be connected to the power supply.

2 Product Structure Diagram



Note: The above diagram shows the block diagram of 100-pin products, some functions of products below 100 pins are not supported.

3 Memory Map


FFFF_FFFFH
Reserved
E010_0000H
E00F_FFFFH
Star Dedicated Peripheral Area
E000_0000H
Reserved
67FF_FFFFH
QSPI
6000_0000H
Reserved
4005_FFFFH
On-Chip Peripheral Area
4000_0000H
Reserved
2001_07FFH
Backup RAM
（2KB）
2001_0000H
2000_FFFFH
RAM
（64KB）
2000_0000H
Reserved
0050_1FFFH
Data Flash
（4KB）
0050_1000H
Reserved
0003_FFFFH
Optical Boot Area
(4KB,8KB,16KB)
0000_0000H
User Flash
(256KB)
67FF_FFFFH
QSPI Register
6400_0000H
63FF_FFFFH
QSPI ROM Window
(64MB)
6000_0000H

4 Pin Functions

4.1 Port functions

4.1.1 64pin products description

(1/3)

Name	I/O	After the reset is released	Multplexing function	Function
PA00	I/O	Analog function	KR0/ANI000/VCIN00/VCIN22/PGA00IN	Port A An 11-bit input/output port, can be designated as an input or output in bit units. Inputs can be set by software using internal pull-up resistors.
PA01			KR1/ANI001/PGA00GND	
PA02			KR2/ANI002/PGA10GND	
PA03			KR4/ANI100/VCIN10/VCIN32/PGA10IN	
PA04			KR5/ANI101/VCIN02/VCIN20/PGA11IN	
PA05			KR6/ANI102/VCIN12/VCIN30/PGA12IN	
PA06			ANI200/PGA12GND	
PA07			ANI201/PGA11GND	
PA08			INTP0/ANI202	
PA09			INTP1/CTxD1/ANI203	
PA10			INTP2/CRxD1/ANI204	
PB00	I/O	Analog function	INTP6/ANI106/TI10/TO10/GTIOC00A/TETRGC	Port B A 7-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PB01			INTP7/ANI212/VCOUT3/TI11/TO11/GTIOC00B/TI06/SPIHS1_NSS/GTETRGD	
PB02			TI02/VCOUT0/ANI213/ANO0/TO06/SPIHS1_SCK/GPTU	
PB03			VCOUT1/ANI214/ANO1/TO02/SPIHS1_MOSI/GPTV	
PB04			VCOUT2/ANI215/TO04/ADTRG2/SPIHS1_MISO/GPTW	
PB05			ANI107/VREF1/TI15/TO15/GTIOC03A/TI04/ADTRG1/GTETRGA	
PB06			TO03/ANI104/GTIOC17A/GTETRGC	
PC00	I/O	Input port	DBD0/GTIOC15B/GTOVLO	Port C A 11-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PC01			DBD1/GTIOC15A/GTOVUP	

(2/3)

Name	I/O	After the reset is released	Multplexing function	Function
PC02			DBD2/GTIOC14B/GTOULO	
PC03			DBD3/GTIOC14A/GTOUUP	
PC04			DBD4/GTIOC12B/GTOWLO	
PC05			DBD5/GTIOC12A/GTOWUP	
PC06			DBD6/GTIOC11B/GTOVLO	
PC07			DBD7/GTIOC11A/GTOVUP	
PC08			GTIOC10B/GTOULO	
PC09			GTIOC10A/GTOUUP	
PC10			INTP4/GTETRGC	
PD00	I/O	Input port	SCLA0/TI12/TO12/GTIOC01A/TI00/SCL21/SCLK21/RxD2/SDI20/SDA20	Port D A 10-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PD01			SDAA0/TI11/TO11/GTIOC00B/SDI21/SDA21/TxD2/SDO20	
PD02			TI10/TO10/GTIOC00A/SDO21/SCLK20/SPIHS1_SCK	
PD03			INTP3/CLKBUZ1/SS10/SDO11/GTETRGD	
PD04			GTIOC02B/TxD1/SDO10/SDI11/SDA11/GTOWLO	
PD05			QSSL/GTIOC02A/RxD1/SDI10/SDA10/SCL11/SCLK11/GTOWUP	
PD06			QIO0/TxD0/SDO00/TO00/SDI01/SDA01/GTETRGC	
PD07			SCLK00/SCL00/QIO1/TI00/TI06/SDO01/GTETRGB	
PD08			RxD0/SDI00/QIO2/SDA00/SCL01/SCLK01/GTETRGA	
PD09			SPIHS0_NSS/QIO3/TO01/TI14/TO14/GTIOC03B/ADST0/SS00/SDO11	

(3/3)

Name	I/O	After the reset is released	Multplexing function	Function
PE00	I/O	Input port	QSPCLK/TI15/TO15/GTIOC03A/TxD1/SDO10/SDI11 /SDA11	Port E A 10-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PE01			NJTRST/GPIO/RTC1HZ/GTETRGA	
PE02			JTCK/SWCLK/GPIO/ADST2/GTETRGB	
PE03			JTMS/SWDIO/GPIO	
PE05			JTDO/TRACESWO/GPIO/CLKBUZ0	
PE06			JTDI/GPIO/GTIOC02A/TI17/TO17/ADST0/SS00	
PE07			GTIOC16A/DBWRB/GTOWUP	
PE08			GTIOC16B/DBRDB/GTOWLO	
PE09			INTP5/DBA0/GTETRGD	
PH00	I	Input port	RESET	Port H A 3-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PH01	I/O		X1	
PH02			X2/EXCLK	

Remark:

1. Each pin is set to digital or analog (capable of being set in bits) via Port Mode Control Register x (PMCx).
2. For the description of the multiplexing function, refer to “4.2 Port Multiplexing Function”.

4.1.2 80pin products description

(1/3)

Name	I/O	After the reset is released	Multplexing function	Function
PA00	I/O	Analog function	KR0/ANI000/VCIN00/VCIN22/PGA00IN	Port A A 14-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PA01			KR1/ANI001/PGA00GND	
PA02			KR2/ANI002/PGA10GND	
PA03			KR4/ANI100VCIN10/VCIN32/PGA10IN	
PA04			KR5/ANI101/VCIN02/VCIN20/PGA11IN	
PA05			KR6/ANI102/VCIN12/VCIN30/PGA12IN	
PA06			ANI200/PGA12GND	
PA07			ANI201/PGA11GND	
PA08			INTP0/ANI202	
PA09			INTP1/CTxD1/ANI203	
PA10			INTP2/CRxD1/ANI204	
PA11			KR3/ANI003	
PA12			KR7/ANI103	
PA13			ANI205	
PB00	I/O	Analog function	INTP6/ANI106//TI10/TO10/GTIOC00A/TETRGC	Port B A 10-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PB01			INTP7/ANI212/VCOUT3/TI11/TO11/GTIOC00B/TI06 /SPIHS1_NSS/GTETRGD	
PB02			TI02/VCOUT0/ANI213/ANO0/TO06/SPIHS1_SCK /GPTU	
PB03			VCOUT1/ANI214/ANO1/TO02/SPIHS1_MOSI/GPTV	
PB04			VCOUT2/ANI215/TO04/ADTRG2/SPIHS1_MISO /GPTW	
PB05			ANI107/VREF1/TI15/TO15/GTIOC03A/TI04/ADTRG1 /GTETRGA	
PB06			TO03/ANI104/GTIOC17A/GTETRGC	
PB07			SS30/ANI105/TI16/TO16/GTIOC02B/GTETRGD	
PB08			ANI007/VREF0/TI14/TO14/GTIOC03B/ADTRG0 /GTETRGB	
PB09			ANI208	

(2/3)

Name	I/O	After the reset is released	Multplexing function	Function
PC00	I/O	Input port	DBD0/GTIOC15B/GTOVLO	Port C A 12-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PC01			DBD1/GTIOC15A/GTOVUP	
PC02			DBD2/GTIOC14B/GTOULO	
PC03			DBD3/GTIOC14A/GTOUUP	
PC04			DBD4/GTIOC12B/GTOWLO	
PC05			DBD5/GTIOC12A/GTOWUP	
PC06			DBD6/GTIOC11B/GTOVLO	
PC07			DBD7/GTIOC11A/GTOVUP	
PC08			GTIOC10B/GTOULO	
PC09			GTIOC10A/GTOUUP	
PC10			INTP4/GTETRGC	
PC11			TI16/TO16/GTIOC03A/SPIHS1_NSS	
PD00	I/O	Input port	SCLA0/TI12/TO12/GTIOC01A/TI00/SCL21/SCLK21/RxD2/SDI20/SDA20	Port D A 13-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PD01			SDAA0/TI11/TO11/GTIOC00B/SDI21/SDA21/TxD2/SDO20	
PD02			TI10/TO10/GTIOC00A/SDO21/SCLK20/SPIHS1_SCK	
PD03			INTP3/CLKBUZ1 SS10/SDO11/GTETRGD	
PD04			GTIOC02B/TxD1/SDO10/SDI11/SDA11/GTOWLO	
PD05			QSSL/GTIOC02A/RxD1/SDI10/SDA10/SCL11/SCLK11/GTOWUP	
PD06			QIO0/TxD0/SDO00/TO00/SDI01/SDA01/GTETRGC	

(3/3)

Name	I/O	After the reset is released	Multplexing function	Function
PD07			SCLK00/SCL00/QIO1/TI00/TI06/SDO01/GTETRGB	
PD08			RxD0/SDI00/QIO2/SDA00/SCL01/SCLK01/GTETRGA	
PD09			SPIHS0_NSS/QIO3/TO01/TI14/TO14/GTIOC03B /ADST0/SS00/SDO11	
PD10			SCL31/SCLK31/TI03/TI14/TO14/GTIOC02A/ADTRG1 /RxD2/SDI20/SDA20/SPIHS1_MISO	
PD11			TI13/SDI31/TO13/SDA31 /GTIOC01B/ TO00/ ADTRG2 /TxD2/SDO20/SPIHS1_MOSI	
PD12			SPIHS0_MOSI/GTIOC00A/TO04/TI01/SCLK10/SCL10 /GTOUUP	
PE00	I/O	Input port	QSPCLK/TI15/TO15/GTIOC03A/TxD1/SDO10/SDI11 /SDA11	Port E A 10-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PE01			NJTRST/GPIO/RTC1HZ/GTETRGA	
PE02			JTCK/SWCLK/GPIO/ADST2/GTETRGB	
PE03			JTMS/SWDIO/GPIO	
PE05			JTDO/TRACESWO/GPIO/CLKBUZ0	
PE06			JTDI/GPIO/GTIOC02A/TI17/TO17/ADST0/SS00	
PE07			GTIOC16A/DBWRB/GTOWUP	
PE08			GTIOC16B/DBRDB/GTOWLO	
PE09			INTP5/DBA0/GTETRGD	
PH00	I	Input port	RESET	Port H A 5-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PH01	I/O		X1	
PH02			X2/EXCLK	
PH03			XT1	
PH04			XT2/EXCLKS	

Remark:

1. Each pin is set to digital or analog (capable of being set in bits) via Port Mode Control Register x (PMCx).
2. For the description of the multiplexing function, refer to “4.2 Port Multiplexing Function”.

4.1.3 100pin products description

(1/4)

Name	I/O	After the reset is released	Multplexing function	Function
PA00	I/O	Analog function	KR0/ANI000/VCIN00/VCIN22/PGA00IN	Port A A 16-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PA01			KR1/ANI001/PGA00GND	
PA02			KR2/ANI002/PGA10GND	
PA03			KR4/ANI100VCIN10/VCIN32/PGA10IN	
PA04			KR5/ANI101/VCIN02/VCIN20/PGA11IN	
PA05			KR6/ANI102/VCIN12/VCIN30/PGA12IN	
PA06			ANI200/PGA12GND	
PA07			ANI201/PGA11GND	
PA08			INTP0/ANI202	
PA09			INTP1/CTxD1/ANI203	
PA10			INTP2/CRxD1/ANI204	
PA11			KR3/ANI003	
PA12			KR7/ANI103	
PA13			ANI205	
PA14			ANI206	
PA15			ANI207	
PB00	I/O	Analog function	INTP6/ANI106/TI10/TO10/GTIOC00A/TETRGC	Port B A 16-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PB01			INTP7/ANI212/VCOUT3/TI11/TO11/GTIOC00B/TI06 /SPIHS1_NSS/GTETRGD	
PB02			TI02/VCOUT0/ANI213/ANO0/TO06/SPIHS1_SCK /GPTU	
PB03			VCOUT1/ANI214/ANO1/TO02/SPIHS1_MOSI/GPTV	
PB04			VCOUT2/ANI215/TO04/ADTRG2/SPIHS1_MISO /GPTW	
PB05			ANI107/VREF1/TI15/TO15/GTIOC03A/TI04/ADTRG1 /GTETRGA	
PB06			TO03/ANI104/GTIOC17A/GTETRGC	
PB07			SS30/ANI105/TI16/TO16/GTIOC02B/GTETRGD	
PB08			ANI007/VREF0/TI14/TO14/GTIOC03B/ADTRG0 /GTETRGB	
PB09			ANI208	
PB10			SDAA1/ANI211	

(2/4)

Name	I/O	After the reset is released	Multplexing function	Function
PB11			SCLA1/ANI210	
PB12			ANI209	
PB13			SCLK30/SCL30/ANI004/TO04/SDO21/GPTU	
PB14			TxD3/SDO30/ANI005/TI04/SDI21/SDA21/GPTV	
PB15			RxD3/SDI30/SDA30/ANI006/SCL21/SCLK21/GPTW	
PC00	I/O	Input port	DBD0/GTIOC15B/GTOVLO	Port C A 16-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PC01			DBD1/GTIOC15A/GTOVUP	
PC02			DBD2/GTIOC14B/GTOULO	
PC03			DBD3/GTIOC14A/GTOUUP	
PC04			DBD4/GTIOC12B/GTOWLO	
PC05			DBD5/GTIOC12A/GTOWUP	
PC06			DBD6/GTIOC11B/GTOVLO	
PC07			DBD7/GTIOC11A/GTOVUP	
PC08			GTIOC10B/GTOULO	
PC09			GTIOC10A/GTOUUP	
PC10			INTP4/GTETRGC	
PC11			TI16/TO16/GTIOC03A/SPIHS1_NSS	
PC12			GTIOC13B/CTxD0/TO02	
PC13			CRxD0/GTIOC13A/TO04/ADTRG0	
PC14			SS20/TO07/TI17/TO17/GTIOC03B	

(3/4)

Name	I/O	After the reset is released	Multplexing function	Function
PC15			TI07/SDO31/TI15/TO15/GTIOC02B/ADTRG0 /SCLK20/SPIHS1_SCK	
PD00	I/O	Input port	SCLA0/TI12/TO12/GTIOC01A/TI00/SCL21/SCLK21 /RxD2/SDI20/SDA20	Port D A 16-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PD01			SDAA0 TI11/TO11/GTIOC00B/SDI21/SDA21/TxD2/SDO20	
PD02			TI10/TO10/GTIOC00A/SDO21/SCLK20/SPIHS1_SCK	
PD03			INTP3/CLKBUZ1/SS10/SDO11/GTETRGD	
PD04			GTIOC02B/TxD1/SDO10/SDI11/SDA11/GTOWLO	
PD05			QSSL/GTIOC02A/RxD1/SDI10/SDA10/SCL11/SCLK11/ GTOWUP	
PD06			QIO0/TxD0/SDO00/TO00/SDI01/SDA01/GTETRGC	
PD07			SCLK00/SCL00/QIO1/TI00/TI06/SDO01/GTETRGB	
PD08			RxD0/SDI00/QIO2/SDA00/SCL01/SCLK01/GTETRGA	
PD09			SPIHS0_NSS/QIO3/TO01/TI14/TO14/GTIOC03B/ADS T0/SS00/SDO11	
PD10			SCL31/SCLK31/TI03/TI14/TO14/GTIOC02A/ADTRG1 /RxD2/SDI20/SDA20/SPIHS1_MISO	
PD11			TI13/SDI31/TO13/SDA31/GTIOC01B/TO00/ADTRG2 /TxD2/SDO20/SPIHS1_MOSI	
PD12			SPIHS0_MOSI/GTIOC00A/TO04/TI01/SCLK10/SCL10 /GTOUUP	
PD13			GTIOC01B/SCLK10/SCL10/GTOVLO	
PD14			SPIHS0_SCK/GTIOC01A/TO06/GTOVUP	
PD15			SPIHS0_MISO/GTIOC00B/TO02/GTOULO	

(4/4)

Name	I/O	After the reset is released	Multplexing function	Function
PE00	I/O	Input port	QSPCLK/TI15/TO15/GTIOC03A/TxD1/SDO10/SDI11/SDA11	Port E A 14-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PE01			NJTRST/GPIO/RTC1HZ/GTETRGA	
PE02			JTCK/SWCLK/GPIO/ADST2/GTETRGB	
PE03			JTMS/SWDIO/GPIO	
PE04				
PE05			JTDO/TRACESWO/GPIO/CLKBUZ0	
PE06			JTDI/GPIO/GTIOC02A/TI17/TO17/ADST0/SS00	
PE07			GTIOC16A/DBWRB/GTOWUP	
PE08			GTIOC16B/DBRDB/GTOWLO	
PE09			INTP5/DBA0/GTETRGD	
PE10			GTIOC17A/TO00/GTETRGA	
PE11			GTIOC17B/TO06/GTETRGB	
PE12			TI05/TI16/TO16/GTIOC02B/TI01/RxD1/SDI10/SDA10/SCL11/SCLK11	
PE13			TO05/TI17/TO17/GTIOC02A/SS10	
PH00	I	Input port	RESET	Port H A 5-bit input/output port, can be designated as an input or output in bit units. The inputs can be set by software using internal pull-up resistors.
PH01	I/O		X1	
PH02			X2/EXCLK	
PH03			XT1	
PH04			XT2/EXCLKS	

Remark:

1. Each pin is set to digital or analog (capable of being set in bits) via Port Mode Control Register x (PMCx).
2. For the description of the multiplexing function, refer to “4.2 Port Multiplexing Function”.

4.2 Port multiplexing function

(1/2)

Name	I/O	Function
ANI000~ANI007, ANI100~ANI107 ANI200~ANI215	I	A/D converter analog inputs
ANO0, ANO1	O	D/A converter outputs
INTP0~INTP7	I	External interrupt request inputs Designation of active edges: rising edge, falling edge, double edges
VCIN00~VCIN03	I	Comparator 0 analog voltage inputs
VCIN10~VCIN13	I	Comparator 1 analog voltage inputs
VCIN20~VCIN23	I	Comparator 2 analog voltage inputs
VCIN30~VCIN33	I	Comparator 3 analog voltage inputs
VREF0	I	Comparator 0 reference voltage inputs
VREF1	I	Comparator 1 reference voltage inputs
VCOUT0~VCOUT3	O	Comparator 0 to 3 outputs
PGA00IN, PGA10IN~PGA12IN	I	PGA00, PGA10 to PGA12 inputs
PGA0GND, PGA10GND~PGA12GND	I	PGA00, PGA10 to PGA12 reference inputs
KR0~KR7	I	Key interrupt inputs
CLKBUZ0, CLKBUZ1	O	Clock outputs/buzzer outputs
RTC1HZ	O	Correction clock (1Hz) output for real-time clock
RESETB	I	A system reset input that is active low and must be connected to V_{DD} either directly or through a resistor when an external reset is not used.
CRxD0, CRxD1, CRxD2	I	CAN serial data inputs
CTxD0, CTxD1, CTxD2	O	CAN serial data outputs
RxD0~RxD3	I	Serial data inputs of serial interfaces UART0, UART1, UART2, and UART3
TxD0~TxD3	O	Serial data outputs of serial interfaces UART0, UART1, UART2, and UART3
SCL00, SCL01, SCL10, SCL11 SCL20, SCL21, SCL30, SCL31	O	Serial clock outputs of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, and IIC31
SDA00, SDA01, SDA10, SDA11 SDA20, SDA21, SDA30, SDA31	I/O	Serial data inputs/outputs of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, and IIC31
SCLK00, SCLK01, SCLK10, SCLK11 SCLK20, SCLK21, SCLK30, SCLK31	I/O	Serial clock inputs/outputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, and SSPI31
SDI00, SDI01, SDI10, SDI11 SDI20, SDI21, SDI30, SDI31	I	Serial data inputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, and SSPI31
SS00	I	Serial interface chip select inputs of SSPI00
SDO00, SDO01, SDO10, SDO11 SDO20, SDO21, SDO30, SDO31	O	Serial data outputs of SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, and SSPI31
DBD0~DBD7	I/O	LCD bus data inputs/outputs

DBRDB	O	LCD bus read enable outputs
DBWRB	O	LCD bus write enable outputs
SCLA0, SCLA1	I/O	Clock inputs/outputs for serial interfaces IICA0 and IICA1
SDAA0, SDAA1	I/O	Serial data inputs/outputs for serial interfaces IICA0 and IICA1

(2/2)

Name	I/O	Function
SPIHS0_NSS	I	Chip select inputs for serial interface SPIHS0
SPIHS0_SCK	I/O	Serial clock inputs/outputs for serial interface SPIHS0
SPIHS0_MISO	I/O	Serial data inputs/outputs for serial interface SPIHS0
SPIHS0_MOSI	I/O	Serial data inputs/outputs for serial interface SPIHS0
SPIHS1_NSS	I	Chip select inputs for serial interface SPIHS1
SPIHS1_SCK	I/O	Serial clock inputs/outputs for serial interface SPIHS1
SPIHS1_MISO	I/O	Serial data inputs/outputs for serial interface SPIHS1
SPIHS1_MOSI	I/O	Serial data inputs/outputs for serial interface SPIHS1
TI00~TI07	I	External count clock/capture trigger inputs for 16-bit Timer80
TO00~TO07	O	Timer outputs for 16-bit Timer80
TI10~TI17	I	External count clock/capture trigger inputs for 16-bit Timer81
TO10~TO17	O	Timer outputs for 16-bit Timer81
GTIOCA00~GTIOCA03, GTIOCB00~GTIOCB03	I/O	Input and output pins for 32-bit general-purpose PWM timer
GTIOCA10~GTIOCA17, GTIOCB10~GTIOCB17	I/O	Input and output pins for 16-bit general-purpose PWM timer
QIO0~QIO3	I/O	QSPI data I/O
QSPCLK	O	QSPI clock outputs
QSSL	O	QSPI slave selection
X1, X2	—	Connect the resonator used for the main system clock.
EXCLK	I	External clock inputs for main system clock
XT1, XT2	—	Connect the resonator used for the subsystem clock.
EXCLKS	I	External clock inputs for subsystem clock
VDD0~VDD3	—	Power supply pin
VSS0~VSS4	—	Ground pin
AVDD0~AVDD2	—	Analog power pin
AVSS0~AVSS2	—	Analog ground level pin
NJTRST	I	JTAG-reset pin
JTCK	I	JTAG-clock pin
JTMS	I	JTAG-TMS signal pin
JTDO	O	JTAG-data output pin
JTDI	I	JTAG-data input pin
SWDIO	I/O	SWD-data interface
SWCLK	I	SWD-clock interface
TRACESWO	O	SWD-TRACE interface

Remark: As a countermeasure against noise and lockup, a bypass capacitor (about 0.1uF) must be connected between V_{DD} and V_{SS} at the shortest possible distance and with thicker wiring.

5 Function Summary

5.1 STAR-MC1 core with ARM® V8-M architecture

This product is equipped with the STAR-MC1 processor, based on ARM® V8-M architecture developed by ARM China. Optimized for IoT devices, the Star processor achieves efficient computation through balanced performance and power consumption configurations. It fully meets IoT device requirements for real-time control, digital signal processing, secure operation, ultra-low power consumption, and compact footprint. For more details, please refer to ARM documentation.

The STAR-MC1 processor integrated in this product includes a Memory Protection Unit (MPU) supporting 8 regions for hardware-managed memory protection, controlling access permissions. It also features CoreSight for debugging and tracing, supporting JTAG or 2-wire Serial Wire Debug (SWD) connections, multi-processor support, and real-time tracing. Users benefit from enhanced debugging capabilities, optimized exception handling, and faster bug localization.

The BAT32G439 utilizes an embedded ARM core, ensuring compatibility with all ARM tools and software.

5.2 Memory

5.2.1 Flash memory

The BAT32G439 has built-in flash memory that can be programmed, erased, and rewritten. It has the following functions:

- Programs and data share 256K storage.
- 4KB dedicated data Flash memory.
- Support page erase, the size of each page is 512byte, erase time is 4ms.
- Support byte/half-word/word (32bit) programming, and programming time is 30μs.

5.2.2 SRAM

The BAT32G439 contains 64KB of embedded SRAM.

5.3 Enhanced DMA controller

It has a built-in enhanced DMA (Direct Memory Access) controller that enables data transfer between memories without using the CPU.

- DMA can be started via peripheral function interrupts, enabling real-time control through communication, timers, and A/D.
- The transfer source/target field is optional for the full address space range (when the flash field is used as the target address, flash needs to be preset as the programming mode).
- Support 4 modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode).

5.4 Linkage controller

The linkage controller links the output events by each peripheral function with the peripheral function trigger sources. This enables collaborative operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- It can link event signals together to realize the linkage of peripheral functions.
- There are 163 types of event input and 33 types of event triggering.

5.5 Clock generation and startup

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits.

5.5.1 Main system clock

- X1 oscillation circuit: The resonator can be connected to pins (X1 and X2) to generate a clock oscillation of 1~20MHz, and the oscillation can be stopped by executing a deep sleep command or setting MSTOP.
- High-speed on-chip oscillator (high-speed OCO): Oscillation can be performed by selecting the frequency by the option byte. After released, the CPU starts running at this high-speed on-chip oscillator clock by default. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed on-chip oscillator. The maximum frequency is 64MHz with an accuracy ±1.0%.
- Input external clock from pin (X2): (1~20MHz), and the input of the external main system clock can be invalidated by executing a deep sleep command or setting the MSTOP bit.

5.5.2 Subsystem clock

- XT1 oscillator circuit: A 32.768kHz clock oscillation can be generated by connecting a 32.768kHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- An external clock input by the pin (XT2): 32.768kHz, and the external clock input can be disabled by setting the XTSTOP bit.

5.5.3 Low-speed on-chip oscillator clock

- Low-speed on-chip oscillator (low-speed OCO): generate a 15kHz (TYP.) clock oscillation. The low-speed on-chip oscillator clock cannot be used as the CPU clock. Only the following peripheral hardware can run off the low-speed on-chip oscillator clock.
- Watchdog timer (WWDT/IWDT)
- Real time clock (RTC)
- 15-bit interval timer

5.5.4 PLL clock

- PLL: can be used as a system clock, the source clock of PLL can be selected from a external clock or an on-chip high-speed oscillator clock.

5.6 Power management

5.6.1 Power supply mode

V_{DD}: External power supply, voltage range: 2.5 to 5.5V.

5.6.2 Power-on reset

The power-on reset circuit (POR) has the following functions.

- An internal reset signal is generated when power is applied. If the MCU voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- Compare the MCU voltage (V_{DD}) and the detection voltage (V_{POR}), when $V_{DD}<V_{POR}$, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode or set to the reset state by the voltage detection circuit or external reset before falling below the operating voltage range. If operation is to be restarted, it must be verified that the power supply voltage has returned to within the operating voltage range.

5.6.3 Voltage detection

The voltage detection circuit sets the operating mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- Compare the MCU voltage (V_{DD}) and the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generate an internal reset or interrupt request signal.
- The detection voltage of the MCU voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by the option bytes.
- Can run in deep sleep mode.
- When the power supply rises, it must be maintained in the reset state by voltage detection circuit or an external reset before reaching the operating voltage range. When the power supply drops, it must be switched to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuit or external reset.
- The operating voltage range varies depending on the setting of the user option bytes.

5.7 Low-power mode

The BAT32G439 supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources:

- Sleep mode: Sleep mode is entered by executing the sleep instruction. Sleep mode is a mode to stop the CPU running clock. If the high-speed system clock oscillator circuit or the high-speed on-chip oscillator is oscillating before the sleep mode is set, each clock continues to oscillate. Although this mode does not allow the operating current to be reduced to the level of deep sleep mode, it is an effective mode when processing is to be restarted immediately by an interrupt request or when frequent intermittent operation is to be performed.
- Deep sleep mode: Deep sleep mode is entered by executing the deep sleep instruction. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillator and high-speed on-chip oscillator and stops the whole system. The operating current of the chip can be greatly reduced. Since the deep sleep mode can be canceled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, since it is necessary to wait for the oscillation to stabilize when releasing the deep sleep mode, it is necessary to select the sleep mode if it is necessary to start processing immediately by an interrupt request.
- Deep sleep mode with partial power down: A deep sleep mode that further reduces power consumption by shutting down part of the peripheral power supply in the deep sleep mode. The deep sleep mode with partial power down is allowed by a pre-configured PMUKEY instruction and executed by a deep sleep instruction. In this mode, PMUCTL can be used to control whether the CPU, CacheRAM, RAM0, RAM1 and Flash are turned off when the oscillator stops oscillating, and most of the peripheral modules will be turned off. Partial power-down deep sleep mode can be released by external interrupts, key-in interrupts, RTC interrupts, 15-bit interval interrupts and WDT/IWDT interrupt requests, so intermittent operation is also possible.

In any of the modes except the deep sleep mode with partial power down, the registers, flags and data memory all remain as they were before being set to standby mode, and the state of the output latches and output buffers of the input/output ports are also maintained. Partial power-down deep sleep mode requires reinitialization of peripheral module functions when it is released.

5.8 Reset function

The following seven methods generate a reset signal.

(1) An external reset is input via the RESETB pin.

(2) The program utilizes watchdog timers for internal reset as a means of detecting and responding to program instability.

(3) An internal reset is generated by comparing the supply voltage and the detection voltage of the power-on reset (POR) circuit.

(4) An internal reset is generated by comparing the supply voltage and the detection voltage of the voltage detection circuit (LVD).

(5) An internal reset occurs due to a RAM parity error.

(6) An internal reset occurred due to access to illegal memory.

(7) Software reset

The internal reset is the same as the external reset, and after the reset signal is generated, the procedure is executed from the addresses written in addresses 0000H and 0001H.

5.9 Interrupt function

The processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 240 interrupt request (IRQ) inputs, one non-maskable interrupt (NMI) input, and multiple internal exceptions. In addition, the processor supports multiple internal exceptions.

The product can support up to 202 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

		64 pins	80 pins	100 pins
Maskable interrupt	External	16	16	16
	Internal	165	175	185

5.10 Real-time clock (RTC)

Functions of real-time clock (RTC) are show as below.

- Having counters of year, month, week, day, hour, minute, and second
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz
- Support prescalers of subsystem clock or main system clock as RTC operation clocks.
- Real-time clock interrupt signals (INTRTC) can be used to wake up in deep sleep mode.
- Watch error correction with high accuracy

Year, month, week, day, hour, minute and second counters are only available if the subsystem clock (32.768kHz) or main system clock prescaler is selected as the RTC operation clock. When the low-speed on-chip oscillator clock (15kHz) is selected, only the constant-period interrupt function can be used.

5.11 Watchdog timer

The BAT32G439 is equipped with two watchdog timers, one for the normal watchdog timer WWDT, one for the independent watchdog timer IWDT, IWDT has the same function as WWDT, but its action is set by the option byte (00404H), WWDT is set to run by the count of the option byte (00400H), and the watchdog timer runs at a low speed on-chip oscillator clock (15KHz). The watchdog timer runs on a low-speed internal oscillator clock (15KHz).

The following are judged to be program instability:

- When the watchdog timer counter overflows
- When a bit operation instruction is executed on the watchdog timer enable register (WDTE)
- When writing data other than “ACH” to the WDTE register
- When writing data to the WDTE register during window closure

5.12 SysTick timer

This timer is exclusive to real-time operating systems, but can also be used as a standard decrement counter.

It is characterized by the generation of a maskable system interrupt when the 24-bit decrementing counter self-loading capacity counter reaches zero.

5.13 General-purpose PWM timer (GPT)

This product includes the GPT0 unit (with 4 channels of 32-bit each) and the GPT1 unit (with 8 channels of 16-bit each). It supports various PWM control waveform generation modes for DC brushless motors:

(1) Sawtooth wave PWM output function
(2) Sawtooth wave pulse mode output function
(3) Triangle wave PWM mode 1 output function
(4) Triangle wave PWM mode 2 output function
(5) Triangle wave PWM mode 3 output function
(6) Synchronous PWM output function
(7) Three-phase complementary PWM output function
(8) Sawtooth wave three-phase complementary PWM output function with automatic dead time setting
(9) Triangle wave three-phase complementary PWM output function
(10) Triangle wave three-phase complementary PWM output function with automatic dead time
(11) Asymmetric triangle wave three-phase complementary PWM output function with automatic dead time

5.14 Timer8

This product has two built-in Timer8 units containing eight 16-bit timers, each of which is referred to as a “channel” and can be used as a stand-alone timer or in combination with multiple channels for advanced timer functions.

5.14.1 Independent channel operation function

The independent channel operation function is a function that allows you to use any channel independently of other channel operation modes. The independent channel operation function is used in the following modes:

(1) Interval timer: It can be used as a reference timer for generating interrupts at fixed intervals (INTTM).

(2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered to output a 50% duty cycle square wave from the timer output pin (TO).

(3) External event counter: Count the effective edge of the input signal of the timer input pin (TI) and can be used as an event counter to generate an interrupt if the specified number of times is reached.

(4) Measurement of input pulse interval: The interval between input pulses is measured by starting counting at the effective edge of the input pulse signal at the timer input pin (TI) and capturing the count value at the effective edge of the next pulse.

(5) High/low width measurement of input signal: Measure the high or low width of the input signal by starting counting on one edge of the input signal of the timer input pin (TI) and capturing the count value on the other edge.

(6) Delay counter: Starts counting at the effective edge of the input signal at the timer input pin (TI) and generates an interrupt after an arbitrary delay period has elapsed.

5.14.2 Multi-channel linkage operation function

The multi-channel linkage operation function is a function that combines the master channel (the reference timer for the main control period) and the slave channel (the timer that follows the operation of the master channel). The multi-channel linkage function can be used in the following modes:

1) Single trigger pulse output: Two channels are used in pairs to generate a single trigger pulse that can arbitrarily set the output timing and pulse width.

2) PWM (Pulse Width Modulation) output: Two channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.

3) Multiple PWM (Pulse Width Modulation) output: Up to 7 PWM signals of any duty cycle can be generated at a fixed period by expanding the PWM function and using one master channel and multiple slave channels.

5.14.3 8-bit timer operation function

The 8-bit timer operation function uses the 16-bit timer channel as the function of two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.15 15-bit interval timer

This product has a built-in 15-bit interval timer that generates interrupts (INTIT) at any pre-set time interval, which can be used to wake up from deep sleep mode.

5.16 Clock output/buzzer output controller

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. The clock output or buzzer output is realized by dedicated pins.

5.17 Universal serial communication unit

This product has 4 built-in general-purpose serial communication units, each unit has up to 4 serial communication channels. It can realize standard SPI, simplified SPI, UART and simplified I^2C communication functions. Take the 100pin product as an example, the functions of each channel are assigned as follows:

5.17.1 3-wire serial interface (SSPI)

Data is transmitted and received synchronously with the serial clock (SCK) output of the master device.

This is a clock-synchronous communication interface that communicates using a total of three communication lines: one serial clock (SCK), one transmit serial data (SO), and one receive serial data (SI).

[Data transmission and reception]

- Data length of 7 to 16 bits
- Phase control of data transmission and reception
- MSB/LSB first

[Clock control]

- Master or slave selection
- Phase control of input/output clock
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Master communication: Max. $F_{CLK}/2$

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

5.17.2 SPI with slave chip selection

This is a clock-synchronous communication interface that communicates using a slave chip select input (SS), a serial clock (SCK), a transmit serial data (SO), and a receive serial data (SI) for a total of four communication lines.

[Data transmission and reception]

- Data length of 7 to 16 bits
- Phase control of data transmission and reception
- MSB/LSB first

[Clock control]

- Phase control of input/output clocks
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

5.17.3 UART

This function enables asynchronous communication over two lines, serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines, data is transmitted and received asynchronously (using the internal baud rate) with other communicating parties in the data frame (consisting of start bits, data, parity bits, and stop bits). Full-duplex UART communication can be implemented by using two channels, dedicated transmitting (even channels) and dedicated receiving (odd channels), and LIN-bus can also be supported by combining a Timer8 unit and an external interrupt (INTP0).

[Data transmission and reception]

- Data length of 7, 8, 9 or 16 bits
- MSB/LSB first
- Level setting for transmitting and receiving data, selection of inversion
- Parity bit appending, parity check function
- Stop bit appending, stop bit detection

[Interrupt function]

- Transfer end interrupt, buffer null interrupt
- Error interrupts caused by frame errors, parity check errors, or overflow errors

[Error detection flag]

- Frame errors, parity errors, overflow errors

[LIN-bus function].

- Detection of wake-up signals
- Detection of break fields (BF)
- Measurement of synchronous fields, calculation of baud rate

5.17.4 Simplified I²C

It is a function to synchronize clock communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Since this simplified I²C is designed for single communication with devices such as Flash memory, and A/D converters, it is used only as a master device. The start and stop conditions, like the operation control registers, must comply with the AC characteristics and are handled by the software.

[Data transmission and reception]

- Master transmission, master reception (limited to the master function of single master)
- ACK output function, ACK detection function
- 8-bit data length (when transmitting the addresses, specify the addresses with the highest 7 bits, and use the lowest bit for R/W control)
- Start and stop conditions are generated by software

[Interrupt function]

- Transfer end interruption

[Error detection flag]

- ACK error, overflow error

[Simplified I²C unsupported features]

- Slave transmission, slave reception
- Multi-master function (arbitration failure detection function)
- Wait detection function

5.18 Standard serial interface SPI

The serial interface SPI has the following 2 modes.

1) Run stop mode: This is the mode used when serial transfer is not in progress, and reduces power consumption.
2) 3-wire serial I/O mode: This mode transfers 8-bit or 16-bit data to and from multiple devices via the 3 wires of the serial clock (SCK) and serial data buses (MISO and MOSI).

5.19 Standard serial interface IICA

This product is equipped with a serial interface IICA, supports slave dual address, and has the following three modes.

(1) Run-stop mode

This is the mode used when serial transfer is not performed, which reduces power consumption.

(2) I^2C bus mode (support multi-master)

This mode transmits 8-bit data to multiple devices over 2 wires of a serial clock (SCLA) and a serial data bus (SDAA). In accordance with the I^2C bus format, the master device can generate “start conditions”, “address”, “indication of transmission direction”, “data” and “stop conditions” on the serial data bus for the slave devices. The slave device automatically detects the received status and data by hardware. This feature simplifies the I^2C bus control part of the application program. Since the SCLA and SDAA pins of the serial interface IICA are used as open drain outputs, pull-up resistors are required for the serial clock line and the serial data bus.

(3) Wake-up mode

In deep sleep mode, when an extension code or a local station address is received from the master device, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). This is set via the IICA control register.

5.20 Synchronous Queued Serial Interface (QSPI)

The 1-channel Quad SPI is designed to connect to a serial ROM (non-volatile memory, such as serial flash, serial EEPROM or serial FeRAM) with an SPI-compatible interface:

- Support extended SPI, dual SPI, quad SPI protocols.
- Configurable for SPI mode 0 and mode 3
- Address width: 8, 16, 24, 32 bits
- Timing is configurable to support various serial flash configurations
- Flash read functions: support read, fast read, fast read dual output, fast read dual I/O, fast read quad output and fast read quad I/O command
- Flexible software-controlled support for a variety of serial flash commands and functions, including erase, write, ID read, and power-down control

5.21 Controller CAN

This product can support up to two general-purpose CAN bus interfaces.

5.22 LCD bus interface

The LCD bus interface has the following functions:

- Support two different bus standards: mode8080, mode6800
- Support 8-bit/16-bit read/write operations
- Controllable transfer speed (up to 10MHz)
- DMA transfer can be triggered when internal data transfer is enabled or external bus access is completed.
- Support DMA read and write

5.23 Analog-to-digital converter (ADC)

This product consists of three 12-bit successive approximation A/D converter units (S12AD0, S12AD1, S12AD2) that convert analog inputs to digital values. Unit 0 supports 8-channel ADC analog inputs (AN000~AN007), Unit 1 supports 8-channel ADC analog inputs (AN100~AN107), and Unit 2 supports 16-channel ADC analog inputs (AN200~AN215).

The A/D converter contains the following functions.

- 12-bit resolution, conversion rate: 1.42Msps.
- Trigger modes: support software trigger, hardware trigger and hardware trigger in standby mode.
- Channel selection: support single-channel select mode and multi-channel scann mode.
- Conversion modes: support single conversion and continuous conversion
- Operating voltage: support operating voltage range: 2.5V≤V_{DD}≤5.5V.
- It can detect the built-in reference voltage (1.45V) and temperature sensors.

The ADC can set various A/D conversion modes by combining the modes described below.

Trigger mode	Software trigger	Start the conversion by operating the software.
	Synchronous trigger	Synchronous triggering selected by the linkage controller. (TRGA0N~TRGA8N, TRGA25N~TRGA28N)
	Asynchronous trigger	The A/D conversion can be triggered by external trigger pins ADTRG0 (S12AD0), ADTRG1 (S12AD1) or ADTRG2 (S12AD2), and the three units can be triggered independently.
Operation mode	Single scan mode	A/D conversion is performed only once for an arbitrarily selected analog input. A/D conversion is performed only once for the internal reference voltage/temperature sensor (S12AD2).
	Continuous scan mode	Repeatedly performs A/D conversion for any selected analog input.
	Group scan mode	The analog inputs selected arbitrarily are divided into two groups (Group A and Group B) or three groups (Group A, B and Group C), and the analog inputs of each group are converted to A/D only once. (When the number of groups is 2, only the combination of groups A and B can be selected.) Group A, B, and C scanning start conditions (synchronous trigger) can be selected independently, so that each group can start A/D conversion independently.
	Group scan mode (when group priority control is selected)	If a high priority group trigger signal is detected during the scanning of a low priority group, the scanning of the low priority group is stopped and the scanning of the priority group is started. The order of priority is group A (highest) > group B > group C (lowest). It is selectable whether to restart the scanning of the low priority group after the processing of the high priority group is completed.

		And it is possible to set the rescanning to start from the starting channel or from the channel where the A/D conversion is not completed.
Sampling time/conversion time	Number of sampling clocks/conversion clocks	The sampling time can be set by registers, the default value of sampling clock number is 13 clk, and the minimum value of conversion clock number is 32 clk.

5.24 Digital-to-analog converter (DAC)

This product has a built-in 2-channel 8-bit resolution analog-to-digital converter (DAC) that converts digital inputs to analog signals. It has the following features:

- 8-bit resolution D/A converter
- Support two independent analog channel outputs
- R-2R ladder network
- Built-in real-time output

5.25 Programmable Gain Amplifier (PGA)

This product has 4 built-in programmable gain amplifiers (PGA00, PGA10, PGA11, PGA12), of which the outputs of PGA00 can be used as analog inputs of A/D converter S12AD0, the outputs of PGA10, PGA11, PGA12 can be used as analog inputs of A/D converter S12ADC1, and the outputs of PGA00, PGA10, PGA11, PGA12 can also be selected as inputs of the positive side of the comparator module.

Each programmable gain amplifier has the following features.

- Support two modes: pseudo-differential and fully differential.
- In pseudo-differential mode, the feedback resistor to ground can optionally connect to either internal or PGAnGND pins (n=00, 10, 11, 12).
- In fully differential mode, the PGAnGND pin serves as the negative terminal of the PGA (n=00, 10, 11, 12).
- Pseudo-differential mode offers a selection of 16 gain multiples, with settings: 2/2.5/…/3.077/4.444/5/8/10/16/1.
- Fully differential mode offers a selection of 4 gain multiples, with settings: 5/8/10/16.

5.26 Comparator (CMP)

This product features four built-in comparators CMP0~CMP3, with the following functionalities:

- The negative terminal reference of the comparator can select DAC output voltage.
- The negative terminal reference of the comparator can optionally use external pin input.
- The positive terminal of the comparator can select PGA output.
- The positive terminal of the comparator can select external pin input.
- Selectable digital filter bandwidth.
- Output inversion function.
- Comparator results can be output from pins (VCOUT0~VCOUT3).
- Capable of detecting valid edges of comparator output and generating interrupt signals.
- CMP1 in conjunction with Timer8 can output TIMERWINDOW.
- Support positive hysteresis, negative hysteresis, and dual-edge hysteresis for comparators, with hysteresis voltage options of 20mV, 40mV, and 60mV.

5.27 Two-wire serial debug port (SW-DP)

The ARM's SW-DP interface allows connection to the microcontroller via a serial line debugging tool.

5.28 Standard JTAG debug port (JTAG)

ARM's JTAG interface allows connection to the microcontroller via a serial line debugging tool.

5.29 Safety functions

5.29.1 Flash CRC function (high-speed CRC, universal CRC)

Data errors in flash memory are detected by CRC operations.

The following two CRCs can be used for different applications and conditions of use.

- High-speed CRC: In the initialization program, it can stop the CPU and check the whole code flash area at high speed.
- Universal CRC: Can be used for multi-purpose checking during CPU operation, not limited to the code flash area.

5.29.2 RAM parity error detection function

Detect parity error when reading RAM data.

5.29.3 SFR guard function

Prevent rewriting of important SFRs (Special Function Registers) due to loss of CPU control.

5.29.4 Illegal memory access detection function

Detect illegal access to an illegal memory area (an area with no memory or an area with restricted access).

5.29.5 A/D test function

The A/D converter is self-tested by A/D converting the positive (+) reference voltage, the negative (-) reference voltage, the analog input channel (ANI), the temperature sensor output voltage, and the internal reference voltage.

5.29.6 Digital output signal level detection function for input/output ports

When the input/output port is in output mode, the output level of the pin can be read.

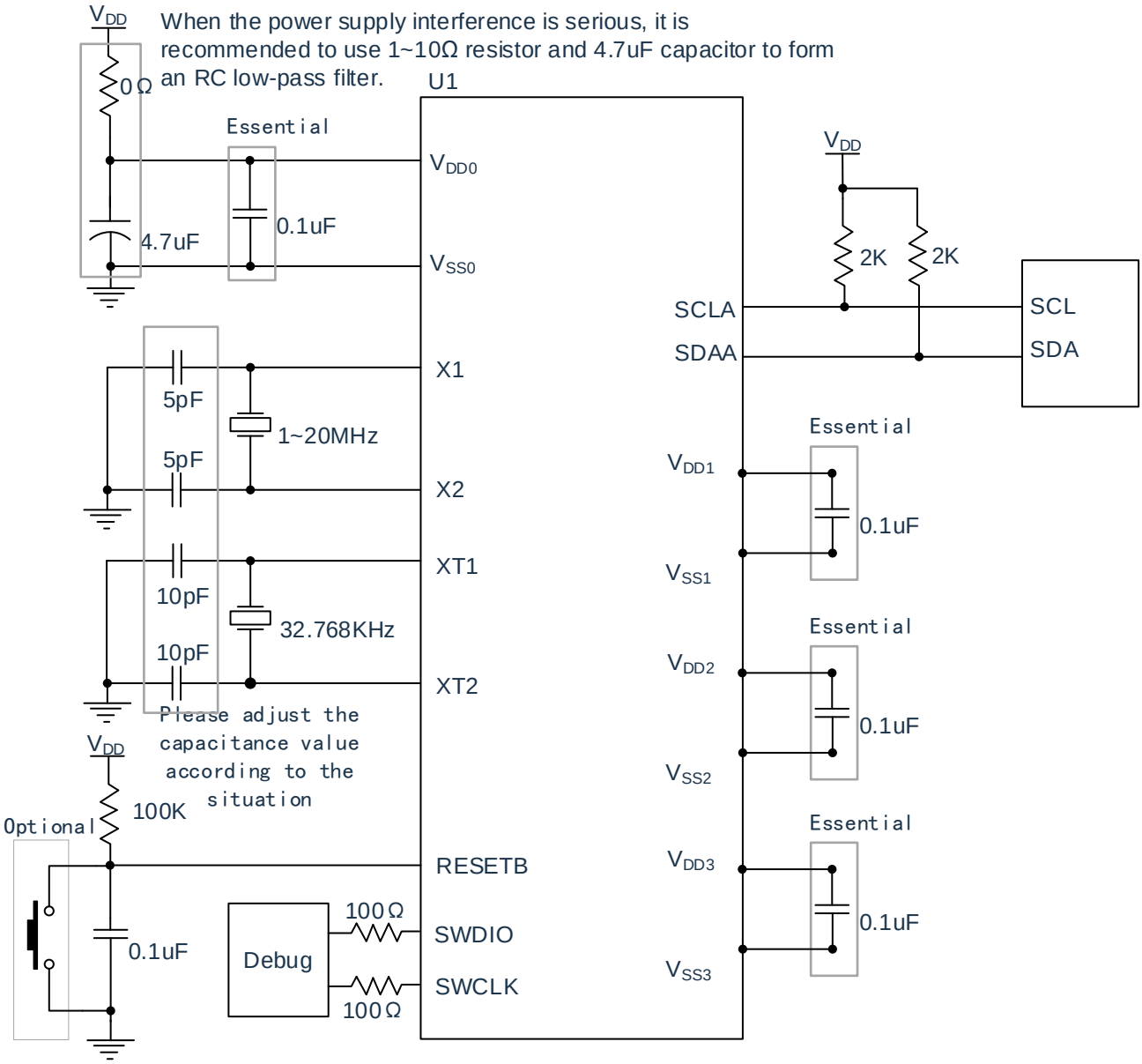
5.30 Key function

A key interrupt (INTKR) can be generated by inputting the falling edge of the key interrupt input pins (KR0~KR7).

6 Electrical Characteristics

6.1 Typical application peripheral circuits

The reference diagram for the connection of peripheral circuits for typical MCU applications is as follows:



6.2 Absolute maximum voltage ratings

(T_A= -40~105°C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	-	-0.5~+6.5	V
Input voltage	V_{I1}	PA00~PA15, PB00~PB15, PC00~PC15 PD00~PD15, PE00~PE13, PH00~PH04	-0.3~V_{DD}+0.3[Note1]	V
	V_{I2}	PH01~PH04, EXCLK, EXCLKS, RESETB	-0.3~V_{DD}+0.3[Note1]	V
Output voltage	V_{O1}	PA00~PA15, PB00~PB15, PC00~PC15 PD00~PD15, PE00~PE13, PH00~PH04	-0.3~V_{DD}+0.3[Note1]	V
Analog input voltage	V_{AI1}	ANI000~ANI007	-0.3~AVDD0+0.3[Note1,2]	V
	V_{AI2}	ANI100~ANI107	-0.3~AVDD0+0.3[Note1,2]	V
	V_{AI2}	ANI200~ANI215	-0.3~AVDD0+0.3[Note1,2]	

Note1: Not more than 6.5V.

Note2: The pin of the A/D conversion object cannot exceed AV_{REF}(+)(AVDD0)+0.3.

Caution: Even if one item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the threshold that can cause physical damage to the product, and it must be operated within this limit.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. AV_{REF}(+): A/D converter positive (+) reference voltage AVDD0 pin level
3. Use V_{SS} as the reference voltage.
4. Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.3 Absolute maximum current ratings

(T_A= -40~105˚C)

Item	Symbol	Condition		Rating	Unit
Output current, high	I_{OH1}	Per pin	PA00~PA15, PB00~PB15, PC00~PC15 PD00~PD15, PE00~PE13	-40	mA
		Pin total -170mA	PA00~PA15, PB00~PB15, PC00~PC15 PD00~PD15, PE00~PE13	-100	mA
	I_{OH2}	Per pin	PH00~PH04	-3	mA
		Pin total		-15	mA
Output current, low	I_{OL1}	Per pin	PA00~PA15, PB00~PB15, PC00~PC15 PD00~PD15, PE00~PE13	40	mA
		Pin total 170mA	PA00~PA15, PB00~PB15, PC00~PC15 PD00~PD15, PE00~PE13	100	mA
	I_{OL2}	Per pin	PH00~PH04	15	mA
		Pin total		45	mA
Operating ambient temperature	T_A	Usually runtime		-40~105	˚C
		When programming the flash memory			
Storage temperature	T_{stg}	-		-65~150	˚C

Caution: Even if one item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the threshold that can cause physical damage to the product, and it must be operated within this limit.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.4 Oscillation circuit characteristics

6.4.1 X1 and XT1 characteristics

(T_A= -40~105℃, 2.5V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
X1 clock oscillation frequency (F_X)	Ceramic/crystal resonator	-	1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic/crystal resonator	20MHz, C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic/crystal resonator	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT})	Crystal resonator	-	32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz, C=10pF	-	2	-	s

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the instruction execution time should be referred to the AC characteristics.
2. Please ask the resonator manufacturer to evaluate the circuit after installation, and use it after confirming the oscillation characteristics.
3. Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.4.2 On-chip oscillator characteristics

(T_A= -40~105℃, 2.5V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (F_{IH}) Note1,2	-	2.0	-	64.0	MHz
High-speed on-chip oscillator stabilization time (T_{SU})	-	-	12	-	us
Clock frequency accuracy of high-speed on-chip oscillator	T_A=10~70℃	-	-	±1.0	%
	T_A=0~105℃	-	-	±1.5	%
	T_A= -10~105℃	-		±2.0	%
	T_A= -40~105℃	-		±4.0	%
Low-speed on-chip oscillator clock frequency (F_{IL})	-	-	15	-	KHz
Low-speed on-chip oscillator clock frequency accuracy	-	-	-	±10	%

Note1: Select the frequency of the high-speed on-chip oscillator via the option byte.

Note2: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.4.3 PLL oscillator characteristics

(T_A= -40~105℃, 2.5V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
PLL input frequency Note1	-	8.0	-	16.0	MHz
PLL lock time	-	40	-	-	μs

Note1: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

6.5 DC characteristics

6.5.1 Pin characteristics

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, high[Note1]	I_{OH1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13 Per pin	2.5V≤V_{DD}≤5.5V -40~85℃	-	-	-12.0[Note2]	mA
			2.5V≤V_{DD}≤5.5V 85~105℃	-	-	-6.0[Note2]	
		Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	-140	mA
			4.0V≤V_{DD}≤5.5V 85~105℃	-	-	-60	
			2.5V≤V_{DD}<4.0V			-30	
	I_{OH2}	PH01~PH04 Per pin	2.5V≤V_{DD}≤5.5V	-	-	2.5	mA
		Total (when duty cycle≤ 70%[Note3])	2.5V≤V_{DD}≤5.5V	-	-	10	mA

Note1: This is the value of current that guarantees the operation of the device even if current flows from the V_{DD} pins to the output pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the “Duty cycle ≤ 70% condition”.

The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (when the duty cycle is changed to n%).

Total pin output current=(I_{OH}×0.7)/(n×0.01)

<Calculation example> I_{OH} = -10.0mA, n =80%

Total pin output current = (-10.0×0.7)/(80×0.01) ≈ -8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Caution: In N-channel open-drain mode, the pin that is set to N-channel open-drain active does not output a high level.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, low[Note1]	I_{OL1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13 Per pin	2.5V≤V_{DD}≤5.5V -40~85℃	-	-	30[Note2]	mA
			2.5V≤V_{DD}≤5.5V 85~105℃	-	-	15[Note2]	
		PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13 Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V -40~85℃	-	-	150	mA
			4.0V≤V_{DD}≤5.5V 85~105℃	-	-	80	
			2.5V≤V_{DD}<4.0V	-	-	50	mA
	I_{OL2}	PH01~PH04 Per pin	2.5V≤V_{DD}≤5.5V	-	-	6[Note2]	mA
		Total (when duty cycle≤ 70%[Note3])	2.5V≤V_{DD}≤5.5V	-	-	20	mA

Note1: This is the value of the current that guarantees the operation of the device even if current flows from the output pins to the V_{SS} pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the “Duty cycle ≤ 70% condition”.

The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (n% duty cycle).

Total output current = (I_{OL}×0.7)/(n×0.01)

<Calculation example> I_{OL}= 10.0mA, n = 80%

Total output current = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply input voltage	V_{DD}	-		2.5	-	5.5	V
Power ground input voltage	V_{SS}	-			-		V
Input voltage, high	V_{IH1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	Schmitt input	0.8V_{DD}	-	V_{DD}	V
	V_{IH2}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	TTL input 4.0V≤V_{DD}≤5.5V	2.2	-	V_{DD}	V
			TTL input 3.3V≤V_{DD}＜4.0V	2.0	-	V_{DD}	V
			TTL input 2.5V≤V_{DD}＜3.3V	1.5	-	V_{DD}	V
	V_{IH3}	PH00~PH04, EXCLK, EXCLKS, RESETB		0.8V_{DD}		V_{DD}	V
	V_{IH4}				-		V
	V_{IH5}				-		V
Input voltage, low	V_{IL1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	Schmitt input	0	-	0.2V_{DD}	V
	V_{IL2}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	TTL input 4.0V≤V_{DD}≤5.5V	0	-	0.8	V
			TTL input 3.3V≤V_{DD}＜4.0V	0	-	0.5	V
			TTL input 2.5V≤V_{DD}＜3.3V	0	-	0.32	V
	V_{IL3}	PH00~PH04, EXCLK, EXCLKS, RESETB		0		0.2V_{DD}	V
	V_{IL4}	-			-		V
	V_{IL5}	-			-		V

Caution: Even in the N-channel open-drain mode, the maximum value of V_{IH} of the pin that is set to be valid for N-channel open-drain is V_{DD}.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.

2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	4.0V≤V_{DD}≤5.5V I_{OH1}= -12.0mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V I_{OH1}= -6.0mA	V_{DD}-0.7	-	-	V
			2.5V≤V_{DD}≤5.5V I_{OH1}= -3.0mA	V_{DD}-0.6	-	-	V
			2.5V≤V_{DD}≤5.5V I_{OH1}= -2mA	V_{DD}-0.5	-	-	V
	V_{OH2}	PH01~PH04	4.0V≤V_{DD}≤5.5V I_{OH2}= -2.5mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V I_{OH2}= -1.5mA	V_{DD}-0.7	-	-	V
			2.5V≤V_{DD}≤5.5V I_{OH2}= -0.5mA	V_{DD}-0.6	-	-	V
			2.5V≤V_{DD}≤5.5V I_{OH2}= -0.4mA	V_{DD}-0.5	-	-	V
Output voltage, low	V_{OL1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	4.0V≤V_{DD}≤5.5V I_{OL1}=35.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL1}=20.0mA	-	-	0.7	V
			2.5V≤V_{DD}≤5.5V I_{OL1}=9.0mA	-	-	0.4	V
			2.5V≤V_{DD}≤5.5V I_{OL1}=7.0mA	-	-	0.4	V
	V_{OL2}	PH01~PH04	4.0V≤V_{DD}≤5.5V I_{OL2}=10.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL2}=6.0mA	-	-	0.7	V
			2.5V≤V_{DD}≤5.5V I_{OL2}=2.5mA	-	-	0.4	V
			2.5V≤V_{DD}≤5.5V I_{OL2}=2.0mA	-	-	0.4	V

Caution: In N-channel open-drain mode, the pin that is set to N-channel open-drain active does not output a high level.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	V_I=V_{DD}	-	-	1	μA
	I_{LIH2}	PH00~PH04 (X1, X2 EXCLK, XT1, XT2, EXCLKS)	V_I=V_{DD}, when the input port and external clock are inputting	-	-	1	μA
			V_I=V_{DD}, when connecting the resonator	-	-	10	μA
Input leakage current, low	I_{LIL1}	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	V_I=V_{SS}	-	-	-1	μA
	I_{LIL2}	PH00~PH04 (X1, X2 EXCLK, XT1, XT2, EXCLKS)	V_I=V_{SS}, when the input port and external clock are inputting	-	-	-1	μA
			V_I=V_{SS}, when connecting the resonator	-	-	-10	μA
Internal pull-up resistance	R_U	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	V_I=V_{SS}, when inputting a port	10	30	100	kΩ
Internal pull-down resistance	R_D	PA00~PA15, PB00~PB15 PC00~PC15, PD00~PD15 PE00~PE13	V_I=V_{SS}, when inputting a port	10	30	100	kΩ

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.5.2 Power supply current characteristics

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Power supply current Note1	I_{DD1}	Run mode	High-speed on-chip oscillator	F_{HOCO}=16MHz, F_{PLL}=128MHz Note3		-	12	40	mA
				F_{HOCO}=64MHz,F_{IH}=64MHz Note3		-	7.5	30	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	6	20	
				F_{HOCO}=24MHz,F_{IH}=24MHz		-	5.5	18	
			High-speed main system clock	F_{MX}=20MHz Note2	Square wave input	-	5.0	13.5	mA
					Crystal oscillator connection	-	5.5	14.5	
			Subsystem clock operation	F_{SUB}=32.768KHz Note4	Square wave input	-	0.25	5.0	mA
					Crystal oscillator connection	-	0.25	5.0	
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	F_{HOCO}=16MHz, F_{PLL}=128MHz Note3		-	6	30	mA
				F_{HOCO}=64MHz, F_{IH}=64MHz Note3		-	3.5	25	
				F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	2.5	16	
				F_{HOCO}=24MHz, F_{IH}=24MHz		-	2.2	14	
			High-speed main system clock	F_{MX}=20MHz Note2	Square wave input	-	1.0	7.5	mA
					Crystal oscillator connection	-	1.5	8.5	
			Subsystem clock operation	F_{SUB}=32.768KHz Note5	Square wave input	-	0.15	4.5	mA
					Crystal oscillator connection	-	0.15	4.5	
		Deep sleep mode Note7	T_A= -40℃~105℃ V_{DD}=3.0V			-	0.15	4.0	mA
	I_{DD3} Note6	Deep sleep mode with partial power	T_A= -40℃~25℃ V_{DD}=3.0V				20	50	μA
			T_A= -40℃~85℃ V_{DD}=3.0V			-	20	500	
			T_A= -40℃~105℃ V_{DD}=3.0V			-	20	750	

		down[Note 7]					

Note1: This is the total current through V_{DD0} to V_{DD3}. Typical alue: The CPU is in multiplication instruction execution (I_{DD1}), and does not include peripheral operating current. Maximum value: The CPU is in multiplication instruction execution (I_{DD1}) and contains external operating current, but does not include current to the A/D converter, LVD circuit, I/O ports, and internal pull-up or pull-down resistors, nor does it include the current when overwriting the data flash memory.

Note2: This is when the high-speed on-chip oscillator and the subsystem clock stop oscillating.

Note3: This is when the high-speed main system and the subsystem clock stop oscillating.

Note4: This is when the high-speed on-chip oscillator and the high-speed main system clock stop oscillating.

Note5: This is when the high-speed on-chip oscillator and the high-speed main system clock stop oscillating. Contains current to the RTC, but does not include current to 15-bit interval timers and watchdog timers.

Note6: Current to RTC, 15-bit interval timers, and watchdog timers is not included.

Note7: For the current value when the subsystem clock is running in deep sleep mode, refer to the current value when the subsystem clock is running in sleep mode.

Remark:

1. F_{HOCO}: High-speed on-chip oscillator clock frequency, F_{IH}: High-speed on-chip oscillator system clock frequency.
2. F_{SUB}: External subsystem clock frequency (XT1/XT2 clock oscillation frequency)
3. F_{MX}: External main system clock frequency (X1/X2 clock oscillation frequency)
4. The typical temperature condition is T_A=25℃.
5. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Low speed on-chip oscillator operating current	I_{FIL} Note1	-		-	0.2	-	μA
RTC operating current	I_{RTC} Note1,2,3	-		-	0.04	-	μA
15-bit interval timer operating current	I_{IT} Note1,2,4	-		-	0.02	-	μA
Watchdog timer operating current	I_{WDT} Note1,2,5	F_{IL}=15KHz		-	0.22	-	μA
A/D converter operating current	I_{ADC} Note1,6	ADC US mode @128MHz		-	2.2	-	mA
		ADC HS mode @4MHz		-	1.3	-	mA
D/A converter operating current	I_{DAC} Note1,8	Per channel		-	0.2	-	mA
PGA operating current		Per channel		-	480	700	μA
Comparator operating current	I_{CMP} Note1,9	Per channel	No internal reference voltage is used	-	60	100	μA

			An internal reference voltage is used	-	80	140	μA
LVD operating current	I_{LVD} Note1,7		-	-	0.08	-	μA

Note1: This is the current flowing through V_{DD}.

Note2: This is when the high-speed on-chip oscillator and the high-speed system clock stop oscillating.

Note3: This is the current that flows only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillation circuit). In the case of a real-time clock operating in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{RTC} value. In addition, I_{FIL} must be added when selecting a low-speed on-chip oscillator. I_{DD2} when the subsystem clock is running contains the operating current of the real-time clock.

Note4: This is the current that flows only to the 15-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and XT1 oscillation circuit). In the case of 15-bit interval timer operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{IT} value. In addition, I_{FIL} must be added when selecting a low-speed on-chip oscillator.

Note5: This is the current that flows only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). In the case of watchdog timer operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus I_{WDT}.

Note6: This is the current that only flows to the A/D converter. In the case of A/D converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{ADC} value.

Note7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{LVD}.

Note8: This is the current that only flows to the D/ A converter. In the case of D/ A converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{DAC} value.

Note9: This is the current that only flows to the comparator circuit. In the case of comparator circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the I_{CMP} value.

Remark:

1. F_{IL}: Low-speed on-chip oscillator clock frequency
2. The typical temperature condition is T_A=25℃.
3. Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.6 AC characteristics

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (F_{MAIN}) is running	2.5V≤V_{DD}≤5.5V	0.015625	-	1	μs
		Subsystem clock (F_{SUB}) is running	2.5V≤V_{DD}≤5.5V	28.5	30.5	31.3	μs
External system clock frequency	F_{EX}	2.5V≤V_{DD}≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	2.5V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
High/low widths of external system clock inputs	T_{EXH}, T_{EXL}	2.5V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS}, T_{EXLS}	2.5V≤V_{DD}≤5.5V		13.7	-	-	μs
TI00~TI07 TI10~TI17 input high/low level width	T_{TIH}, T_{TIL}	2.5V≤V_{DD}≤5.5V		1/F_{MCK}+ 10	-	-	ns

Remark:

1. F_{MCK}: Timer8 unit operating clock frequency
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output frequencies of TO00 ~ TO03 TO10 ~ TO17 TAIO0, TAO0 TMIOA0, TMIOA1 TMIOB0, TMIOB1 TMIOC0, TMIOC1 TMIOD0, TMIOD1 TBIOA, TBIOB	F_{TO}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.5V≤V_{DD}<4.0V		-	-	8	MHz
Output frequencies of CLKBUZ0, CLKBUZ1	F_{PCL}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.5V≤V_{DD}<4.0V		-	-	8	MHz
High/low widths of interrupt inputs	T_{INTH} T_{INTL}	INTP0 ~ INTP7	2.5V≤V_{DD}≤5.5V	1	-	-	μs
High/low level widths of key interrupt inputs	T_{KR}	KR0 ~ KR7	2.5V≤V_{DD}≤5.5V	250	-	-	ns
Low-level width of RESETB	T_{RSL}	-		10	-	-	μs

6.7 Peripheral function characteristics

6.7.1 Universal interface unit

(1) UART mode

(T_A= -40~85℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.5V ≤ V_{DD} ≤ 5.5V	-	-	F_{MCK}/6	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	10.6	Mbps

(T_A=85~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.5V ≤ V_{DD} ≤ 5.5V	-	-	F_{MCK}/12	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	5.3	Mbps

Remark: It is guaranteed by the design, and is not tested in mass production.

(2) 3-wire SPI mode (master mode, internal clock output)

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		-40~85℃		85~105℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY1}	$T_{KCY1} \geqslant 2/F_{CLK}$	4.0V ≤ V_{DD} ≤ 5.5V	31.25	-	62.5	-	ns
			2.7V ≤ V_{DD} ≤ 5.5V	41.67	-	83.33	-	ns
			2.5V ≤ V_{DD} ≤ 5.5V	65	-	125	-	ns
SCLKp high/low level width	T_{KH1} T_{KL1}	4.0V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-4	-	T_{KCY1}/2-7	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-5	-	T_{KCY1}/2-10	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-10	-	T_{KCY1}/2-20	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK1}	4.0V ≤ V_{DD} ≤ 5.5V		12	-	23	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V		17	-	33	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V		20	-	38	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI1}	2.5V ≤ V_{DD} ≤ 5.5V		5	-	10	-	ns
Delay time from SCLKp↓→SDOp	T_{KSO1}	2.5V ≤ V_{DD} ≤ 5.5V C=20pF Note1		-	5	-	10	ns

Note1: C is the load capacitance of the SCLKp, SDOp output lines.

Caution: Through the Port Input Mode Register and Port Output Mode Register, the SDIp pin is selected as the normal input buffer and the SDOp pin and SCLKp pin are selected as the normal output mode.

Remark: It is guaranteed by the design, and is not tested in mass production.

(3) 3-wire SPI mode (slave mode, external clock input)

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz＜F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤20MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz＜F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V		6/F_{MCK} and ≥ 500	-	12/F_{MCK} and≥ 1000	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK2}	2.7V ≤ V_{DD} ≤ 5.5V		1/F_{MCK} +20	-	1/F_{MCK} +40	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V		1/F_{MCK} +30	-	1/F_{MCK} +60	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI2}	2.5V ≤ V_{DD} ≤ 5.5V		1/F_{MCK} +31	-	1/F_{MCK} +62	-	ns
Delay time from SCLKp↓→ SDOp	T_{KSO2}	2.7V ≤ V_{DD} ≤ 5.5V C=30pF Note1		-	2/F_{MCK} +44	-	2/F_{MCK} +66	ns
		2.5V ≤ V_{DD} ≤ 5.5V C=30pF Note1		-	2/F_{MCK} +75	-	2/F_{MCK} +113	ns

Note1: C is the load capacitance of the SCLKp, SDOp output lines.

Caution: Through the Port Input Mode Register and Port Output Mode Register, the SDIp and SCLKp pins are selected as the normal input buffers and the SDOp pin is selected as the normal output mode.

Remark: It is guaranteed by the design, and is not tested in mass production.

(4) 4-wire SPI mode (slave mode, external clock input)

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min.	Max.	Min.	Max.	
SS00 set-up time	T_{SSIK}	DAPmn=0	2.7V ≤ V_{DD} ≤ 5.5V	120	-	240	-	ns
			2.5V ≤ V_{DD} ≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+ 120	-	1/F_{MCK}+ 240	-	ns
			2.5V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+ 200	-	1/F_{MCK}+ 400	-	ns
SS00 hold time	T_{KSSI}	DAPmn=0	2.7V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+ 120	-	1/F_{MCK}+ 240	-	ns
			2.5V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+ 200	-	1/F_{MCK}+ 400	-	ns
		DAPmn=1	2.7V ≤ V_{DD} ≤ 5.5V	120	-	240	-	ns
			2.5V ≤ V_{DD} ≤ 5.5V	200	-	400	-	ns

Caution: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: It is guaranteed by the design, and is not tested in mass production.

(5) Simplified IIC mode

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	-40 ~ 85℃		85 ~ 105℃		Unit
			Min.	Max.	Min.	Max.	
SCLr clock frequency	F_{SCL}	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	-	1000Note1	-	400Note1	KHz
		2.5V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	-	400Note1	-	100Note1	KHz
		2.5V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	-	300Note1	-	75Note1	KHz
Hold time when SCLr is low	T_{LOW}	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475	-	1200	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1150	-	4600	-	ns
		2.5V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550	-	6500	-	ns
Hold time when SCLr is high	T_{HIGH}	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475	-	1200	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1150	-	4600	-	ns
		2.5V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550	-	6500	-	ns
Data setup time (reception)	$T_{SU:DAT}$	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	1/F_{MCK}+85 Note2	-	1/F_{MCK}+220 Note2	-	ns
		2.5V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1/F_{MCK}+145 Note2	-	1/F_{MCK}+580 Note2	-	ns
		2.5V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1/F_{MCK}+230 Note2	-	1/F_{MCK}+1200 Note2	-	ns
Data hold time (transmission)	$T_{HD:DAT}$	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	-	305	-	770	ns
		2.5V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	-	355	-	1420	ns
		2.5V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	-	405	-	2070	ns

Note1: The value must also be equal to or less than F_{MCK}/4.

Note2: Set the F_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Remark: It is guaranteed by the design, and is not tested in mass production.

6.7.2 Serial interface IICA

(1) I²C standard mode

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLAr clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	4.7	-	μs
Hold time of the start condition Note1	$T_{HD: STA}$	-	4.0	-	μs
Hold time when SCLAr is low	T_{LOW}	-	4.7	-	μs
Hold time when SCLAr is high	T_{HIGH}	-	4.0	-	μs
Data set-up time (reception)	$T_{SU: DAT}$	-	250	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	3.45	μs
Set-up time of the stop condition	$T_{SU: STO}$	-	4.0	-	μs
Bus idle time	T_{BUF}	-	4.7	-	μs

Note1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during ACK.

Remark:

1. The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:
   Standard mode: C_b=400pF, R_b=2.7KΩ
2. It is guaranteed by the design, and is not tested in mass production.

(2) I²C fast mode

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLAr clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz	-	400	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.6	-	μs
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.6	-	μs
Hold time when SCLAr is low	T_{LOW}	-	1.3	-	μs
Hold time when SCLAr is high	T_{HIGH}	-	0.6	-	μs
Data set-up time (reception)	$T_{SU: DAT}$	-	100	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.9	μs
Set-up time of the stop condition	$T_{SU: STO}$	-	0.6	-	μs
Bus idle time	T_{BUF}	-	1.3	-	μs

Note1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note2: The maximum (MAX.) value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during ACK.

Remark:

1. The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:
   Fast mode: C_b=320pF, R_b=1.1KΩ
2. It is guaranteed by the design, and is not tested in mass production.

(3) I²C enhanced fast mode

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLAr clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz	-	1000	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.26	-	μs
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.26	-	μs
Hold time when SCLAr is low	T_{LOW}	-	0.5	-	μs
Hold time when SCLAr is high	T_{HIGH}	-	0.26	-	μs
Data set-up time (reception)	$T_{SU: DAT}$	-	50	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.45	μs
Set-up time of the stop condition	$T_{SU: STO}$	-	0.26	-	μs
Bus idle time	T_{BUF}	-	0.5	-	μs

Note1: Generate the first clock pulse after a start condition or restart condition is generated.

Note2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during ACK.

Remark:

1. The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:
   Enhanced fast mode: C_b=120pF, R_b=1.1KΩ
2. It is guaranteed by the design, and is not tested in mass production.

6.8 Analog characteristics

6.8.1 A/D converter characteristics

(T_A= -40~105℃, 2.5V≤AVDD0≤VDD≤5.5V, V_{SS}=0V; reference voltage (+)=AVDD0, reference voltage (-)=AVSS0=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.5V ≤AVDD0≤ 5.5V	-	-	±4.0	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.5V ≤AVDD0≤ 5.5V	-	-	±4.0	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.5V ≤AVDD0≤ 5.5V	-	-	±4.0	LSB
Integral linearity error Note1	EL	12-bit resolution	2.5V ≤AVDD0≤ 5.5V	-	-	±4.0	LSB
Differential linearity error Note1	ED	12-bit resolution	2.5V ≤AVDD0≤ 5.5V	-	-	±2.0	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion object: ANI2~ANI15	2.5V ≤V_{DD}≤ 5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.5V ≤V_{DD}≤ 5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} ＜ (Ts / (F_{ADC} x C_{ADC} x ln(2^{12+2})) - R_{ADC})		-	3.75 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2		pF
Analog input voltage	V_{AIN}	ANI000~ANI007, ANI100~ANI107, ANI200~ANI215		0	-	AVDD0	V
		Internal reference voltage (2.5V≤V_{DD}≤5.5V)		V_{BGR} Note2			V
		Temperature sensor output voltage (2.5V≤V_{DD}≤5.5V)		V_{TMPS25} Note2			V

Note1: Quantization error (±1/2 LSB) is not included.

Note2: Please refer to “6.8.2 Characteristics of temperature sensor/internal reference voltage”.

Note3: Tmclk is the action clock period of the AD, and the maximum action frequency is 128MHz.

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.2 Characteristics of temperature sensor/internal reference voltage

(T_A= -40~105℃, 2.5V≤V_{DD}≤5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A= -40~105℃	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	μs

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.3 D/A converter

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-	-	-	-	8	bit
Combined error	AINL	Rload=4MΩ	2.5V≤V_{DD}≤5.5V	-	-	±2.5	LSB
Stabilization time	T_{SET}	Cload=20pF	2.7V≤V_{DD}≤5.5V	-	-	3	μs
			2.5V≤V_{DD}<2.7V	-	-	6	μs
Output load	RO	Rload=4MΩ	2.5V≤V_{DD}≤5.5V	4.7		8	KΩ

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.4 Comparator

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input offset voltage	V_{IOCMP}	-	-	±10	±40	mV
Input voltage range	I_{VCMP}	-	0	-	V_{DD}	V
Response time	T_{CR}, T_{CF}	Input amplitude±100mV	-	70	150	ns
Operation stabilization time	T_{CMP}		-	-	3	μs
Operating current	I_{CMPDD}	See 6. 5. 2 Power supply current characteristics				-

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.5 Programmable gain amplifier (PGA)

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input offset voltage	V_{IOPGA}	-		-	-	±10	mV
Input voltage range	V_{IPGA}	-		0	-	0.9xV_{DD}/ Gain	V
Output voltage range	V_{IOHPGA}	-		0.93xV_{DD}	-	-	V
	V_{IOLPGA}	-		-	-	0.07xV_{DD}	V
Gain error	-	In full differential mode	x5	-	-	±1	%
			x8	-	-	±1	
			x10	-	-	±1	
			x16	-	-	±2	
		In pseudo-differential mode	x2.000	-	-	±1	%
			x2.500	-	-	±1	
			x2.667	-	-	±1	
			x2.857	-	-	±1	
			x3.077	-	-	±1	
			x3.333	-	-	±1	
			x3.636	-	-	±1	
			x4.000	-	-	±1	
			x4.444	-	-	±1	
			x5.000	-	-	±1	
			x5.714	-	-	±1	
			x6.667	-	-	±1	
			x8.000	-	-	±1	
			x10.000	-	-	±1	
			x16.000	-	-	±2	
			x1.000	-	-	±1	
Conversion rate	SR_{RPGA}	Rising Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (other than x32)	3.5	-	-	V/μs
			4.0 V ≤ V_{DD} ≤ 5.5 V(x32)	3.0	-	-	
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5	-	-	
	SR_{FPGA}	Falling Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (other than x32)	3.5	-	-	
			4.0 V ≤ V_{DD} ≤ 5.5 V(x32)	3.0	-	-	
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5	-	-	

Stable operation time[Note1]	T_{PGA}	In full differential mode	x5	-	-	5	us
			x8	-	-	5	
			x10	-	-	5	
			x16	-	-	10	
		In pseudo-differential mode	x2.000	-	-	5	us
			x2.500	-	-	5	
			x2.667	-	-	5	
			x2.857	-	-	5	
			x3.077	-	-	5	
			x3.333	-	-	5	
			x3.636	-	-	5	
			x4.000	-	-	5	
			x4.444	-	-	5	
			x5.000	-	-	5	
			x5.714	-	-	5	
			x6.667	-	-	5	
			x8.000	-	-	5	
			x10.000	-	-	5	
			x16.000	-	-	10	
			x1.000	-	-	5	
Operating current	I_{PGADD}	See 6. 5. 2 Power supply current characteristics					

Note1: The time required from the PGA action enable (PGAEN=1) to fulfill each of the DC and AC style requirements of the PGA.

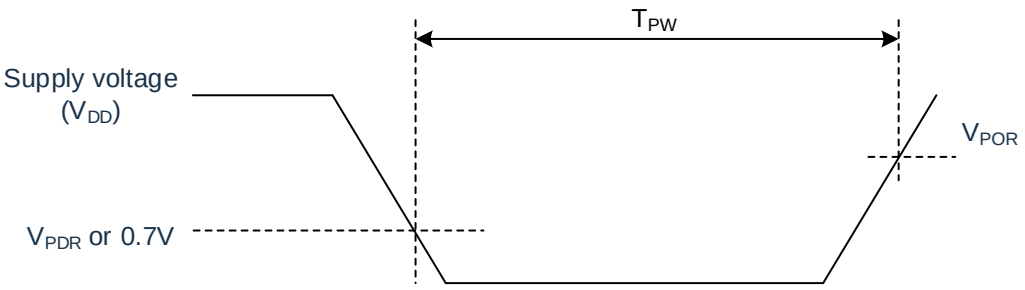
Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.6 POR circuit characteristics

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	V_{POR}	When the supply voltage rises	-	1.50	1.75	V
	V_{PDR}	When the supply voltage drops	1.37	1.45		V
Minimum pulse width Note1	T_{PW}	-	300	-	-	μs

Note1: This is the time required to reset the POR when V_{DD} falls below V_{PDR}. In addition, when the oscillation of the main system clock (F_{MAIN}) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC) in the deep sleep mode, this is the time required for POR reset from the time when V_{DD} is lower than 0.7V to the time when it rises above V_{POR}.



Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.7 LVD circuit characteristics

1. Reset mode, interrupt mode

(T_A= -40~105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.14	V
		When the supply voltage drops	3.90	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.13	-	V
		When the supply voltage drops	-	3.06	-	V
	V_{LVD3}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD4}	When the supply voltage rises	-	2.92	-	V
		When the supply voltage drops	-	2.86	-	V
	V_{LVD5}	When the supply voltage rises	-	2.81	-	V
		When the supply voltage drops	-	2.75	-	V
	V_{LVD6}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD7}	When the supply voltage rises	-	2.61	-	V
		When the supply voltage drops	-	2.55	-	V
	V_{LVD8}	When the supply voltage rises	-	2.50	2.55	V
		When the supply voltage drops	2.40	2.45	-	V
Minimum pulse width	T_{LW}	-	300	-	-	μs
Detection delay	-	-	-	-	300	μs

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

2. Interrupt & reset mode

(T_A= -40~105℃, $V_{PDR} \leqslant V_{DD} \leqslant$5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Detection voltage	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Drop the reset voltage		2.40	2.45	-	V
	V_{LVDC1}		LVIS1=1 LVIS0=0	Rise the reset release voltage	-	2.61	2.66	V
				Drop the interrupt voltage	2.50	2.55	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.71	-	V
				Drop the interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	3.75	-	V
				Drop the interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Drop the reset voltage			2.75		V
	V_{LVDD1}		LVIS1=1 LVIS0=0	Rise the reset release voltage		2.92	-	V
				Drop the interrupt voltage	-	2.86	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	3.02	-	V
				Drop the interrupt voltage	-	2.96	-	V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	4.06	4.14	V
				Drop the interrupt voltage	3.90	3.98	-	V

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.8 Rise slope characteristics of supply voltage

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	T_{RESET}	-	-	1	-	ms
Rising slope of supply voltage	SV_{DD}	-	-	-	54	V/ms

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.9 Memory characteristics

6.9.1 Flash memory

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Symbol	Item	Condition	Min.	Max.	Unit
T_{PROG}	Word program (32bit)	T_A= -40~105℃	-	120	μs
T_{ERASE}	Sector erase (512B)	T_A= -40~105℃	2	3	ms
	Chip erase	T_A= -40~105℃	30	40	ms
N_{END}	Endurance	T_A= -40~105℃	100	-	Kcycle
T_{RET}	Data retention	100Kcycle[Note1] at T_A= 105℃	20	-	year

Note1: Cycling tests are performed over the entire temperature range.

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.9.2 RAM memory

(T_A= -40~105℃, 2.5V≤VDD≤5.5V, VSS=0V)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{RAMHOLD}$	RAM hold voltage	T_A= -40~105℃	0.8	-	V

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.10 EMS characteristics

6.10.1 ESD eletrical characteristics

Symbol	Item	Test condition	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	T_A = 25°C, JESD22-A114	3A

Remark: It is guaranteed by the design, and is not tested in mass production.

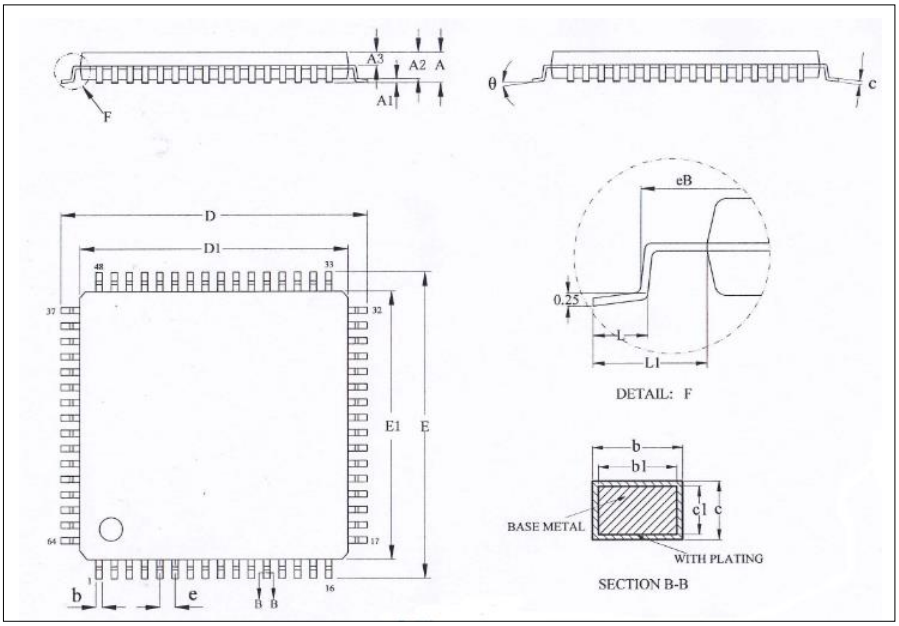
6.10.2 latch-up eletrical characteristics

Symbol	Item	Test condition	Classification
LU	Static latch-up class	T_A = 25°C, JESD78F	IA

Remark: It is guaranteed by the design, and is not tested in mass production.

7 Package

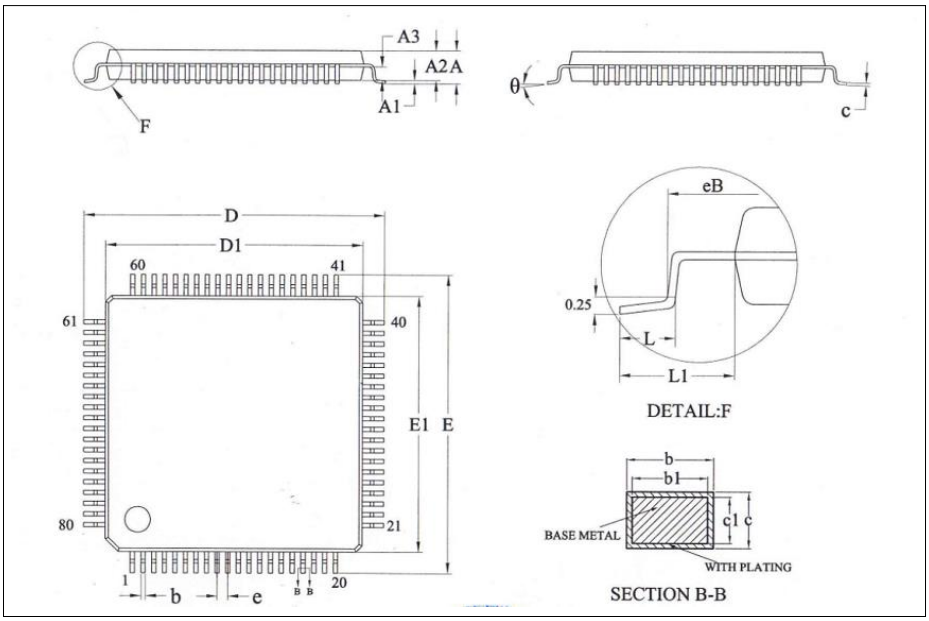
7.1 LQFP64(10x10mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.26
b1	0.17	0.20	0.23
c	0.09	-	0.18
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
eB	11.05	-	11.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

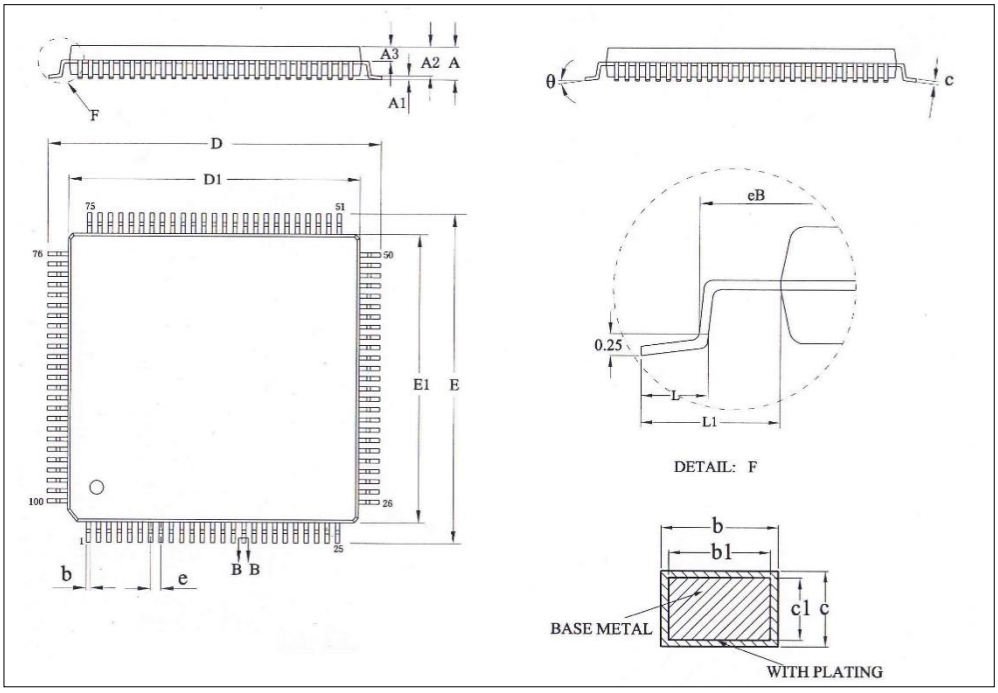
7.2 LQFP80(12x12mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	-	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

7.3 LQFP100(14x14mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.35
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

8 Revision History

Version	Date	Revision content
V0.1.0	March 2023	Initial version
V0.1.1	April 2023	1) Added 1.3 Top view and revised the remarks. 2) Modified 6.1 Typical application peripheral circuits. 3) Features: fixed typo, updated description of low speed oscillator. 4) Features, 1.1 Brief introduction: updated description of operating power consumption 5) 2 Product Structure Diagram: added IWDT function, corrected IrDA multiplexing. 6) 4.1 Port functions: updated VCIN function name and deleted note 3 7) 5.1 STAR-MC1 core with ARM® V8-M architecture, 5.4 Linkage controller, 5.5.3 Low-speed on-chip oscillator clock: corrected content 8) 5.7 Low-power mode: added partial power-down deep sleep mode description 9) 5.11 Watchdog timer: added IWDT 10) 5.17 Universal serial communication unit: corrected data length and deleted “Transmit and receive data level setting”. 11) 5.23 Analog-to-digital converter (ADC), Programmable Gain Amplifier (PGA), 5.26 Comparator (CMP): updated content 12) 6.5.2 Power supply current characteristics: added conditions for the high-speed on-chip oscillator: F_{HOCO}=16MHz, F_{IH}=128MHz 13) 6.8.5 Programmable gain amplifier (PGA): Condition modification and addition of gain deviation and operation stabilization time 14) 5.17 Universal serial communication unit, 6.7.1 Universal interface unit: SPI chip select input changed to SS 15) Updated format
V0.1.2	September 2023	1) Updated LCDB function pin description in section 2: Product Structure Diagram 2) The LCD data bus interface is modified to 8-bit “DBD0~DBD7”, and the pin connection diagram and pin function description are modified accordingly. 3) Corrected PE07 multiplexing function GTIOC16B to GPIOC16A. 4) Modified the format of the pin map 5) Updated ADC error data in section 6.8.1
V0.1.3	February 2024	1) Modified 6.1 Typical application peripheral circuits 2) Modified the XT1 clock oscillation starting capacitance value in 6.4.1 3) Updated TBD parameters in 6.5.2/6.10.2 4) Updated power consumption parameters in deep sleep mode
V0.1.4	September 2024	1) Revised the cover page 2) Modified LQFP64 package dimensions and add remarks for other packages